MOTOROLA
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EP450™

Portable Radio
Detailed Service Manual

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EP450 Portable Radio
Detailed Service Manual

VHF 136-162 MHz
VHF 146-174 MHz
UHF 403-440 MHz
UHF 438-470 MHz
UHF 465-495 MHz
UHF 490-527 MHz

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HKLN4216C

Foreword

This manual is intended for use by service technicians familiar with portable two-way radios. It contains service information required for the equipment described and is current as of the printing date. Changes which occur after the printing date may be incorporated by a complete Manual revision or alternatively as additions

Product Safety and RF Exposure Compliance

Caution

Before using this product, read the operating instructions for safe usage contained in the Product Safety and RF Exposure booklet enclosed with your radio.

ATTENTION!

This radio is restricted to occupational use only to satisfy FCC RF energy exposure requirements. Before using this product, read the RF energy awareness information and operating instructions in the Product Safety and RF Exposure booklet enclosed with your radio (Motorola Publication part number 6881095C98) to ensure compliance with RF energy exposure limits.

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Chapter 1 Test Equipment, Service Aids, and Service Tools

1.1 Test Equipment

Table 1-1 lists test equipment required to service the EP450 Radios.

Table 1-1. Recommended Test Equipment

Motorola Part No.	Description	Characteristics	Application
R2600 series	System analyzer	This item will substitute for items with an asterisk (*)	Frequency/deviation meter and signal generator for wide-range troubleshooting and alignment
*R1074	Fluke 87 digital multimeter	True RMS metering, 200 kHz frequency counter, 32-segment bar graph with backlit display	Digital voltmeter is recommended for AC/DC voltage and current measurements
	Fluke 85 RF probe	500 MHz, 30 VAC max	Use with Fluke 87 digital multimeter for RF voltage measurements.
*R1377	AC voltmeter	1 mV to 300 mV, 10 megaohm input impedance	Audio voltage measurements
R1611	Dual channel 100 MHz oscilloscope (Agillent)	Two-channel, 100 MHz bandwidth, 200 M sample rate/sec, 2 MB memory/channel	Waveform measurements
S1339	RF millivolt meter	100 µV to 3V RF, 10 kHz to 1 GHz frequency range	RF level measurements
*R1013 or *R1370	SINAD meter or SINAD meter with RMS	Without RMS audio voltmeter or With RMS audio voltmeter	Receiver sensitivity measurements

1.2 Service Aids

Table 1-2 lists service aids recommended for working on the EP450 Radios. While all of these items are available from Motorola, most are standard shop equipment items, and any equivalent item capable of the same performance may be substituted for the item listed.

Table 1-2. Service Aids

Motorola Part No.	Description	Application
RLN4460	Portable Test Set	Enables connection to the audio/accessory jack. Allows switching for radio testing.
RLN4510	Battery Interface	Regulates DC current and voltage between radio and power supply.
RVN4195	Customer Programming Software and Tuner Software on CD Rom	Program customer option and channel data.
AAPMKN4004	Programming Test Cable	Connects radio to RIB (RLN4008).
AAPMKN4003	Radio-to-Radio Cloning Cable	Allows a radio to be duplicated from a master radio by transferring programmed data from the master radio to the other.
RLN4008	Radio Interface Box	Enables communications between the radio and the computer's serial communications adapter.
5886564Z01	RF Adaptor	Adapts radio's antenna port to BNC cabling of test equipment.
0180305K08	Shop Battery Eliminator	Interconnects radio to power supply.
HSN9412	Wall-Mounted Power Supply	Used to supply power to the RIB (120 VAC).
3080369B71 or 3080369B72	Computer Interface Cable	Use B72 for the IBM PC AT or newer (9-pin serial port). Use B71 for older models (25-pin serial port). Connects the computer's serial communications adapter to the RIB (PLN4008).
6686533Z01	Knob Remover/Chassis Opener	Used to remove the front cover assembly.
HKN9216	IBM Computer Interface Cable	Connection from computer to RIB.
8180384N65	Housing Eliminator	Allows testing of the radio outside of the housing.
RLN5583	Flashing Adapter	Flashing/CPS cable for Authorized Service Centers

Table 1-3. Recommended Service Tools

Motorola Part No.	Description	Application
RSX4043	TORX screwdriver	Tighten and remove chassis screws
6680387A70	T6 TORX bit	Removable TORX screwdriver bit
R1453	Digital readout solder station	Digitally controlled soldering iron

Table 1-3. Recommended Service Tools (Continued)

Motorola Part No.	Description	Application
RLN4062	Hot air workstation, 120 V	Tool for hot air soldering/desoldering of surface mounted integrated circuits
0180386A78	Illuminated magnifying glass with lens attachment	Illumination and magnification of components
0180302E51	Master lens system	
0180386A82	Anti-static grounding kit	Used during all radio assembly and disassembly procedures
6684253C72	Straight prober	
6680384A98	Brush	
1010041A86	Solder (RMA type), 63/67, 0.5mm diameter, 1 lb. spool	
0180303E45	SMD tool kit (included with R1319A)	
R1319	ChipMaster (110 V)	Surface mount removal and assembly of surface mounted integrated circuits and/or rework station shields. Includes 5 nozzles.
R1321	ChipMaster (220 V)	
ChipMaster Nozzles:		
6680332E83	PLCC-28* nozzle	Soldering and Un-soldering IC's
6680332E82	PLCC-44* nozzle	
6680332E94	PLCC-52 nozzle	
6680332E96	PLCC-84 nozzle	
6680334E67	QFP-160 nozzle	
6680333E46	SOL-18 nozzle	
6680332E84	SOIC-20 nozzle	
6680332E87	SOL-20J nozzle	
6680333E45	SOL-24 nozzle	
6680333E55	TSOP-64 nozzle	

* Included with ChipMaster packages

Programming/Test Cable

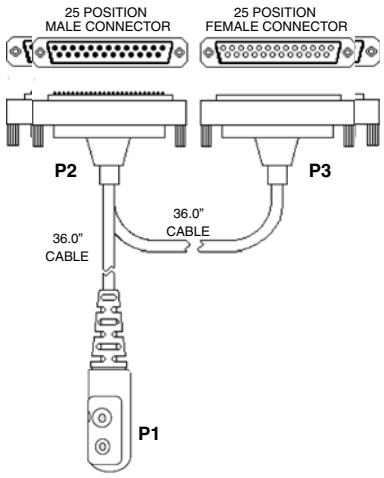

Figure 1-1. Programming/Test Cable

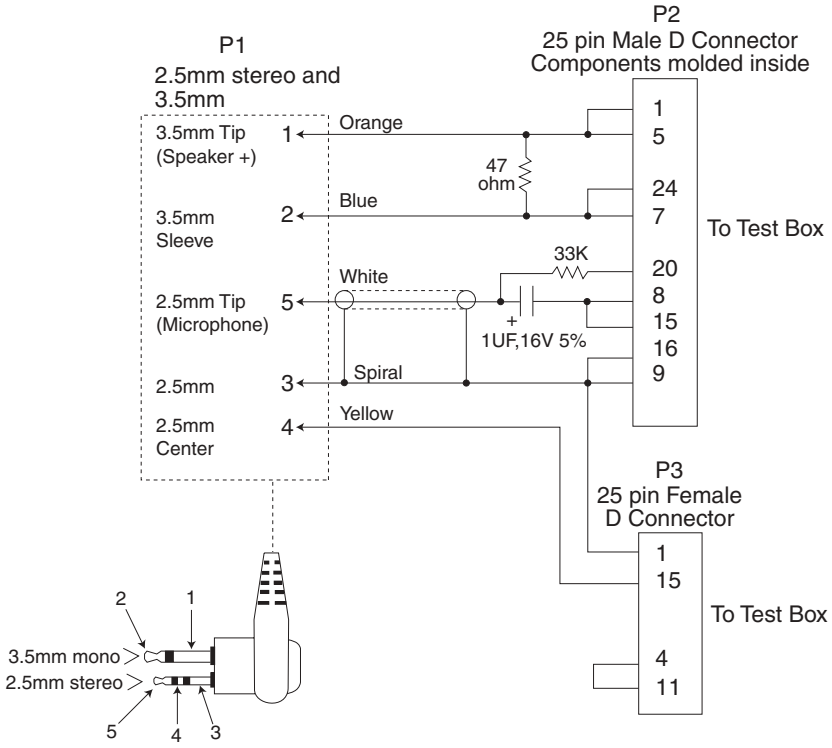

Figure 1-2. Wiring of the Connectors

Chapter 2 DC Power Distribution

2.1 DC Regulation and Distribution

A block diagram of the DC power distribution throughout the radio is shown in Figure 2-1.

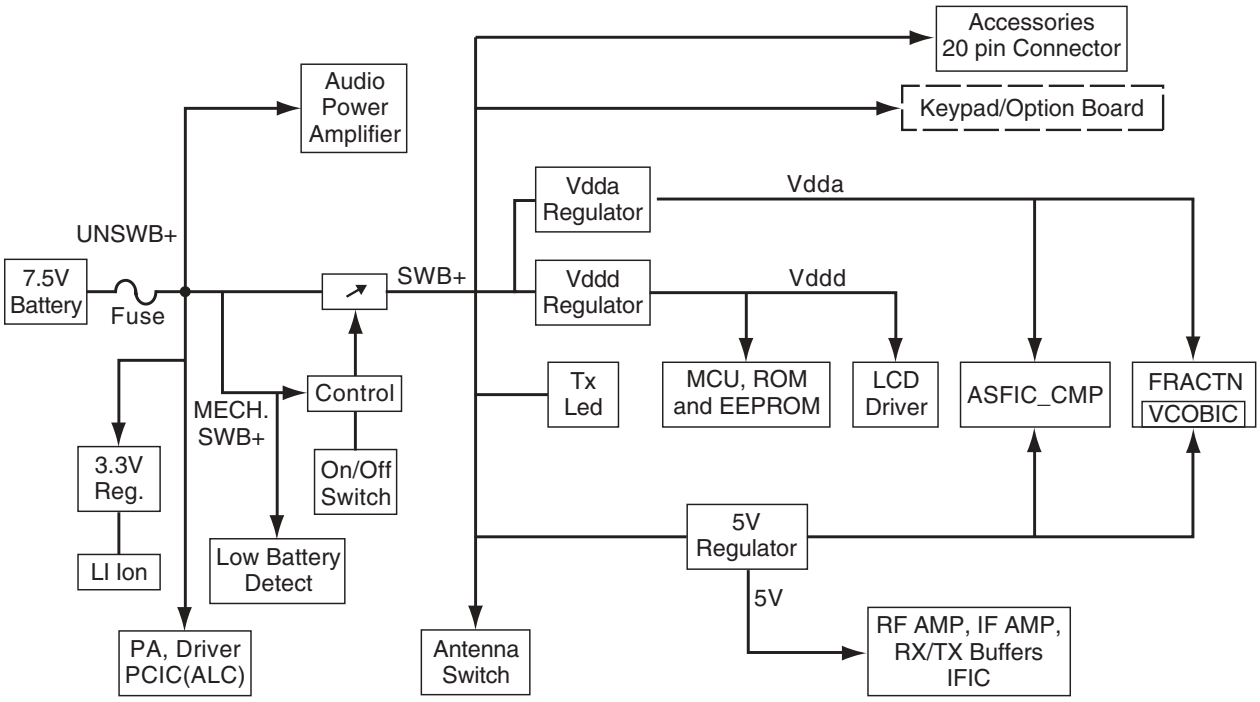

Figure 2-1. DC Power Distribution Block Diagram

Battery voltage enters at connector J301 and is routed through fuse F301 to become USWB+. VR301 protects against ESD, and D301 provides reverse polarity protection. This voltage is routed to:

- FET switch Q170 in the TX power control circuit (turned on during transmit)
- TX power amplifier module U110 (via R150)
- input pins of regulators U310, U320 and U330
- FET switch Q493 (turned on whenever the radio is on)
- on-off switch S444 (part of on-off-volume control) to become SWB+

When the radio is turned on, SWB+ is present and is applied to:

- transistor switch Q494 (pins 1 and 6) which turns on Q493
- RX audio power amplifier U490
- voltage divider R420/R421 and port PE0, a microprocessor A/D input which measures battery voltage and radio on/off status

The output of FET switch Q493 is applied to the control pins of regulators U310, U320 and U330, turning them on. The following regulators are used:

Table 2-1. Voltage Regulators

Reference No.	Description	Type
U310	5 V Regulator	TK71750S
U320	Digital 3.3 V Regulator	LP2986
U330	3 V Regulator	TK71730S

The 5 V source is applied to:

- RX back end circuitry
- synthesizer super filter input and charge pump supply
- RED/GRN LEDs
- RX audio buffer U510
- portions of ASFIC U451

The 5 V source is also applied to FET switches Q311 and Q312. Q311 is turned on by Q313 when RX_ENA (from U401 pin 49) is high, and supplies the “5R” source to the RF front end stages Q21-Q22, and the VCO RX injection buffer Q280. Q312 is turned on by Q313 when TX_ENA (from U401 pin 50) is high, and supplies the “5T” source to the first transmitter stage Q100.

The digital 3.3 volt source from U320 (D_3.3 V) is applied to:

- microprocessor U401
- EEPROM U402
- S-RAM U403
- flash ROM U404

The 3 V regulated source from U330 is applied to:

- synthesizer IC U201
- VCO/buffer IC U251
- portions of ASFIC U451
- microphone bias circuitry

While the radio is turned on, port PH3 (U401 pin 44) is held high. When the radio is turned off, SWB+ is removed and port PE0 (U401 pin 67) goes low, initiating a power-down routine. Port PH3 (pin 44) remains high, keeping the voltage regulators on via Q493 and Q494, until the operating state of the radio has been stored in EEPROM and other turn-off data functions have been completed. PH3 then goes low, turning off Q494 and Q493, and all regulated voltages are removed.

Chapter 3 Controller Theory of Operation

3.1 Controller

The controller provides the following functions:

- interface with controls and indicators
- serial bus control of major radio circuit blocks
- encoding and/or decoding of selective signaling formats such as PL, DPL, MDC-1200 and QuikCall II
- interface to CPS programming via the microphone connector
- storage of customer-specific information such as channel frequencies, scan lists, and signaling codes
- storage of factory tuning parameters such as transmitter power and deviation, receiver squelch sensitivity, and audio level adjustments
- power-up, power-down and reset routines

Figure 7-31 (VHF) shows the interconnection between the controller and the various other radio blocks. Figure 7-37 show the connections between the following circuit areas which comprise the controller block:

- microprocessor circuitry
- audio circuitry
- DC regulation circuitry (refer to Chapter 2, DC Regulations and Distribution.)
- rotary and pushbutton controls and switches
- option board interface

The majority of the circuitry described below is contained in the (VHF) Microprocessor Circuitry schematic diagrams (Figure 7-38). Portions are also found in the Audio and DC Regulation schematics (Figures 7-39 and 7-40).

3.1.1 Microprocessor Circuitry

The microprocessor circuitry includes microprocessor (U401) and associated EEPROM, S-RAM (not used in EP450 models), and Flash ROM memories. The following memory IC's are used:

Table 3-1. Radio Memory Requirements

Reference No.	Description	Type	Size
U402	Serial EEPROM	AT25128	16K x 8
U403	Static RAM	(not used)	
U404	Flash ROM	AT49LV001N_70 V	128K x 8

3.1.1.1 Memory Usage

Radio operation is controlled by software that is stored in external Flash ROM memory (U404). Radio parameters and customer specific information is stored in external EEPROM (U402). The operating status of the radio is maintained in RAM located within the microprocessor. When the radio is turned off, the operating status of the radio is written to EEPROM before operating voltage is removed from the microprocessor. See section "3.1.1.7 Microprocessor Power-Up, Power-Down and Reset Routine" on page 3-3 for a discussion of the power-down routine.

Parallel communication with U403 and U404 is via:

- address lines A(0)-A(16), from U401 port F ADDR0-ADDR13 and port G XA14-XA16
- data lines D(0)-D(7), from U401 port C DATA0-DATA7
- chip-select for U403, from PH6 (U401 pin 41)
- chip-enable for U404, from PH7 (U401 pin 38)
- output enable for U404, from PA7 (U401 pin 86)
- write-enable for both U403 and U404, from PG7_R/W (U401 pin 4)

Serial communication with U402 is via:

- the SPI bus (see section "3.1.1.3 Serial Bus Control of Circuit Blocks" on page 3-2)
- chip-select for U402, from PD6 (U401 pin 3)

3.1.1.2 Control and Indicator Interface

Ports PI3 and PI4 are outputs which control the top-mounted LED indicator. When PI3 is high, the indicator is red. When PI4 is high, the indicator is green. When both are high, the indicator is amber. When both are low, the indicator is off.

Pressing the side-mounted PTT button (S441) provides a low to port PJ0 (U401 pin 71), which indicates PTT is asserted. Side-mounted option buttons 1 and 2 (S442 and S443) are connected to Ports PJ6 (pin 77) and PJ7 (pin 78), respectively.

3.1.1.3 Serial Bus Control of Circuit Blocks

The microprocessor communicates with other circuit blocks via a SPI (serial peripheral interface) bus using ports PD2 (data into uP), PD3 (data out of uP) and PD4 (clock). The signal names and microprocessor ports are defined in Table 3-2.

Table 3-2. SPI Bus Signal Definitions

Signal Name	Microprocessor Port	Microprocessor Pin
SPI-DATA_IN	PD2-MISO	U401 Pin 99
SPI_DATA_OUT	PD3-MOSI	U401 pin 100
SPI_CLK	PD4-SCK	U401 pin 1

These signals are routed to:

- the audio filter IC (U451) to control internal functions such as gain change between 25 kHz and 12.5 kHz channels, transmit or receive mode, volume adjustment, etc.
- the synthesizer IC U201 to load receive and transmit channel frequencies
- option board connector J460-1 for internal option configuration and control
- serial EEPROM U402 (both SPI_DATA_IN and SPI_DATA_OUT are used).

In order for each circuit block to respond only to the data intended for it, each peripheral has its own chip select (or chip enable) line. The device will only respond to data when its enable line is pulled low by one of the microprocessor ports, as follows:

- port PD5 (U401 pin 2) for the audio filter IC
- port PH0 (U401 pin 47) for the synthesizer IC
- port PH4 (U401 pin 43) for the option board/display enable
- port PD6 (U401 pin 3) for the serial EEPROM.

3.1.1.4 Interface to RSS Programming

The radio can be programmed, or the programmed information can be read, using a computer with CPS (Customer Programming Software) connected to the radio via a RIB (radio interface box) or with the RIB-less cable. Connection to the radio is made via the microphone connector (part of accessory connector J471). The SCI line connects the programming contact (J471 pin 6) to ports PD0_RXD (data into uP, pin 97) and PD1_TXD (data out of uP, pin 98). Transistor Q410 isolates the input and output functions by allowing PD1 to pull the line low, but does not affect incoming data from being read by port PD0. This isolation allows high-speed 2-wire programming via TP401 and TP402 for factory programming and tuning.

3.1.1.5 Storage of Customer-Specific Information

Information that has been programmed using CPS, such as channel frequencies or selective signaling codes, are stored in the external EEPROM, where it is retained permanently (unless reprogrammed) without needing DC power applied to the microprocessor.

3.1.1.6 Sensing of Externally-Connected Accessories

Port PJ1 is used to detect the presence of externally connected accessories. Port PJ1 (U401 pin 72) is normally low, unless accessories (lapel speaker microphone, lightweight headset, etc.) are used with the radio. This port is used to detect an accessory PTT or auto sensing of a VOX accessory.

If VOX is programmed into the radio channel codeplug information, and PJ1 is high during power-up, the radio will activate VOX operation. If a low is present at port PJ1 during power-up, the radio will use this port as an external PTT indicator.

3.1.1.7 Microprocessor Power-Up, Power-Down and Reset Routine

On power-up, the microprocessor is held in reset until the digital 3.3 V regulator (U320 pin 5) provides a stable supply voltage. Once the digital supply reaches steady state and releases the reset line (U320 pin 7), the microprocessor begins to start up. The ASFIC_CMP (U451) has already started running and is providing the startup clock to the microprocessor. After reset release by all circuits, the software within the microprocessor begins executing port assignments, RAM checking, and initialization. A fixed delay of 100 ms is added to allow the audio circuitry to settle. Next, an alert beep is generated and the steady state software begins to execute (buttons are read, radio circuits are controlled).

When the radio is turned off, SWB+ is removed and port PE0 (U401 pin 67) goes low, initiating a power-down routine. Port PH3 (pin 44) remains high, keeping the voltage regulators on via Q493 and Q494, until the operating state of the radio has been stored in EEPROM. PH3 then goes low, and all regulated voltages are removed.

The microprocessor reset line (pin 94) can be controlled directly by the digital 3.3 V regulator (U320 pin 7), the microphone jack (part of accessory connector J471) via Q472 and Q471, and the microprocessor itself. U320 pulls the reset line low if the digital 3.3 V source loses regulation. This prevents possible MOS latch-up or overwriting of registers in the microprocessor because the reset line is higher in voltage than the microprocessor VDD ports (U401 pins 12, 39, 59, 88). The microprocessor can drive the reset line low if it detects a fault condition such as an expired watchdog timer, software attempting to execute an infinite loop, unplanned hardware inputs, static discharge, etc. Finally, the Q471 can pull the reset line low during use of the programming cable and CPS by the application of a sufficiently negative voltage to the microphone connector tip contact (J471 pin 4), however this reset method is not utilized.

3.1.1.8 Boot Mode Control

When power-up reset occurs, the microprocessor will boot into either normal or flash mode depending on the logic level of ports MODA (U401 pin 58) and MODB (pin 57). The Flash Adapter is a programming accessory which provides negative 9 volts dc via a 1K resistor to microphone connector J471 pin 4. This turns on Q471 and Q472 via D471 and VR472, pulling MODA and MODB low and allowing booting in the flash mode by cycling power to reset the radio. Software upgrades can then performed by loading the new software code into Flash ROM U404.

3.1.1.9 Microprocessor 7.3975 MHz Clock

The 7.3975 MHz clock signal (uP_CLK) is provided from the ASFIC_CMP (U451 pin 28). Upon startup the 16.8MHz crystal provides the signal to the ASFIC_CMP, which sends out the uP_CLK at 3.8MHz until a steady-state condition is reached and the clock is increased to 7.3975MHz for the microprocessor.

3.1.1.10 Battery Gauge

Various battery types are available having different capacities. The different battery types contain internal resistors connected from the BATT_CHARGE contact to ground (which is routed to the microprocessor as BATT_DETECT). A voltage divider is formed with R255 producing a different DC voltage for each battery type, which is read by microprocessor port PE2 (pin 65). This allows the software to recognize the battery chemistry being used and adjust the battery gauge for best accuracy.

3.1.2 Audio Circuitry

3.1.2.1 Transmit and Receive Low-Level Audio Circuitry

The majority of RX and TX audio processing is performed by U451, the Audio Filter IC (ASFIC_CMP), which provides the following functions:

- Tone PL/Digital PL encode and decode filtering
- Tone PL/Digital PL rejection filter in RX audio path
- TX pre-emphasis amplifier
- TX audio modulation limiter
- Post-limiter (splatter) filter
- TX deviation adjust (digitally-controlled attenuators)
- Programmable microphone gain attenuator
- RX audio volume control (digitally controlled attenuator)
- Carrier squelch adjustment (digitally controlled attenuator)
- Microprocessor output port expansion

- 2.5 volt dc reference source
- Microprocessor clock generation (from the 16.8 MHz reference oscillator input)

The parameters of U451 that are programmable are selected by the microprocessor via the CLOCK (U451 pin 21), DATA (U451 pin 22) and chip enable (U451 pin 20) lines.

RX audio buffer U510 amplifies the audio level from the DEMOD output of the IFIC before being applied to the audio filter IC input (DISC, U451 pin 2). The buffer is DC coupled to avoid corruption of low-frequency data waveforms such as DPL. Because such waveforms are polarity sensitive, this buffer is configured as a single-stage inverting amplifier (U510-1 only) for VHF models where high-side first injection is used, or is configured as a two-stage non-inverting amplifier (U510-1 and -2) for UHF models using low-side first injection. The gain of the buffer is 1.5 times or 3.5 dB.

Volume adjustment is performed by a digital attenuator within U451. The volume control (10KO, part of S444) is connected to D_3.3 V and ground via R506 and R507. When the volume control is rotated, it varies the dc voltage applied to microprocessor A/D input port PE1 (U401 pin 66) between approximately 0 volts dc at minimum volume to 3.3 volts dc at maximum volume. Depending on this voltage, the appropriate setting of the digital volume attenuator is selected. This technique is less susceptible to noise than a conventional analog volume control.

3.1.2.2 Audio Power Amplifier

The audio power amplifier IC U490 amplifies receiver audio from U451 pin 41 to a level sufficient to drive a loudspeaker. U490 is a bridge amplifier delivering 3.46 volts rms between pins 5 and 8 without distortion, which is sufficient to develop 500 milliwatts of audio power into the internal 24 ohm speaker or an external 24 ohm load. The audio power amplifier is muted whenever speaker audio is not required to reduce current drain. The audio amp is muted when U451 pin 14 is low. When U451 pin 14 is high, U490 pin 1 is pulled low by Q490, enabling the audio amplifier.

Because the power amplifier is a bridge-type, neither speaker terminal is grounded. Care should be taken that any test equipment used to measure the speaker audio voltage does not ground either speaker output terminal, otherwise damage to the audio power amplifier IC may result. When a 24-ohm load resistor is used it should be connected between the tip and the sleeve of accessory jack J471 (3.5mm port), never to ground. External SPKR plug insertion mechanically disconnects the internal speaker. Voltage measurements using test equipment that is not isolated from ground may be made from one side of the speaker or load resistor (either the tip or the sleeve of J471) to chassis ground, in which case the voltage indicated will be one half of the voltage applied to the speaker or load resistor. The Motorola RLN4460 Portable Test Set and AAPMKN4004 Programming Test Cable provide the proper interface between the radio's ungrounded audio output and ground-referenced test equipment.

3.1.2.3 Internal Microphone Audio Voice Path

Microphone audio from internal microphone is routed from J470-1 via C475, L471, and C470 to the ASFIC_CMP mic audio input (MICINT, U451 pin 46). During transmit, Q470 is turned on by a low at U451 pin 35, providing dc bias for the internal MIC via R478. External MIC plug insertion mechanically disconnects the internal microphone. External MIC audio is coupled through L471 and C470 to the mic audio input. An input level of 10 mV at J471 pin 4 produces 200 mV at the output of U451 pin 40, which corresponds to 60% deviation.

3.1.2.4 PTT Circuits

The internal side-mounted PTT switch (S441) is sensed directly by microprocessor port PJ0 (U401 pin 71). External mic PTT is sensed by measuring the current drawn through the accessory connector (J471-4) by the mic cartridge (which is in series with the accessory PTT switch). This current is drawn through the base (pin 5) and emitter (pin 4) of a transistor in Q470, causing its collector (pin 3) to supply a logic-high to microprocessor port PJ1 (pin 72).

3.1.2.5 VOX Operation

VOX audio accessories do not have a PTT switch. Instead, the mic cartridge is wired directly from J471-4 to ground. If the radio has been programmed for VOX operation and the VOX accessory is plugged in prior to turning the radio on, the current drawn by the cartridge will turn on Q470 (pins 3-4-5) and a logic high will be seen at port PJ1 at turn-on. The microprocessor then assumes VOX operation, with PTT controlled by the presence of audio at the mic cartridge. A dc voltage proportional to the audio level at the input of the ASFIC_CMP (U451 pin 46) is fed to an A/D input of microprocessor U401 (pin 62). During VOX operation, PTT is activated when the dc level exceeds a preset threshold.

3.1.2.6 Programming and Flashing Through Microphone Jack

The ring contact on the 2.5 mm microphone jack is used for reading, programming or re-flashing the radio using CPS. This contact (J471 pin 6) is routed to ports PD0_RXD (data into uP, pin 97) and PD1_TXD (data out of uP, pin 98). Transistor Q410 isolates the input and output functions by allowing PD1 to pull the line low, but does not affect incoming data from being read by port PD0.

To re-flash the radio (overwrite the software in the Flash ROM with new software), the radio must power up in the boot mode. This is accomplished by using a flash adapter accessory, which provides SCI communication with the programming ring contact (J471 pin 6) and also allows a negative voltage (negative 9 volts dc via a 1K resistor) to be applied to the tip contact (J471 pin 4). This voltage is sufficient to turn on the base-emitter junction (pins 1 and 2) of Q472 via L471, D471, VR472 and R471. Pin 6 of Q472 goes high, turning on Q471 (pins 3 and 4) and pulling the BOOT_ENA line (ports MODA and MODB of the microprocessor) low. Cycling power generates a reset which causes the radio to boot in the flash mode.

Chapter 4 136-162 MHz VHF Theory Of Operation

4.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Chapter 7 of this manual.

4.2 VHF Receiver

The VHF receiver covers the range of 136-162 MHz and provides switchable IF bandwidth for use with 12.5 kHz or 20/25 kHz channel spacing systems. The receiver is divided into two major blocks as shown in Figure 4-1.

- Front End
- Back End

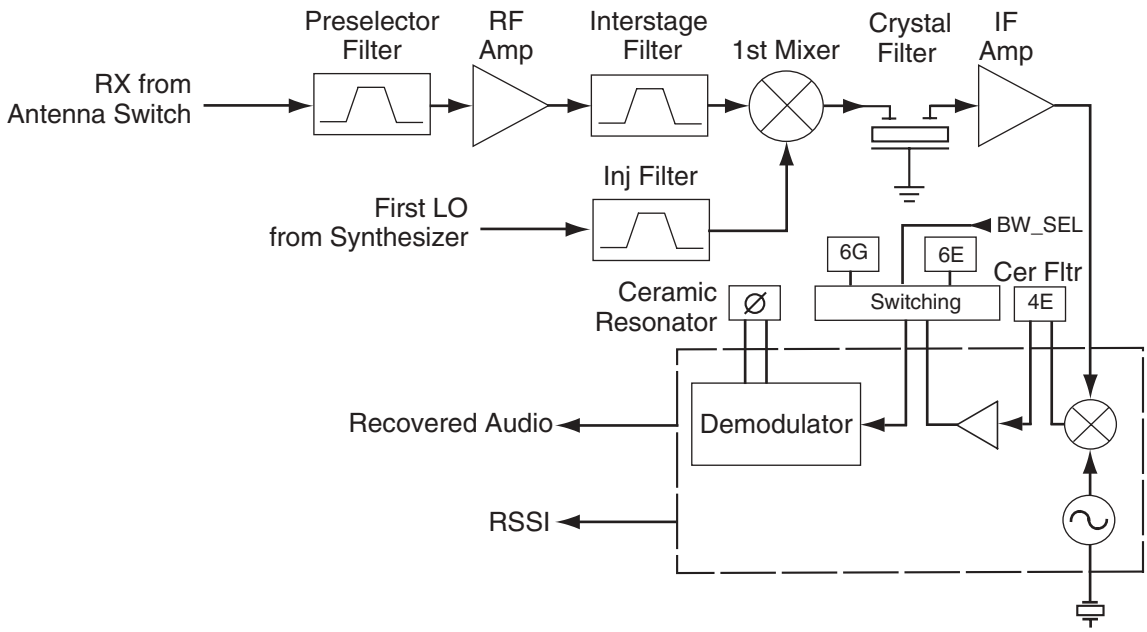

Figure 4-1. VHF Receiver Block Diagram

4.2.1 Receiver Front-End

Incoming RF signals from the antenna are first routed through the harmonic filter and antenna switch, part of the transmitter circuitry, before being applied to the receiver front end. The receiver front end consists of a preselector filter, RF amplifier, an interstage filter, and a double-balanced first mixer.

The preselector filter is a fixed-tuned 4-pole design using discrete elements (L1-L4 and C1-C9) in a series/shunt resonator configuration. It has a 3 dB bandwidth of 43 MHz, an insertion loss of 2 dB and image attenuation of 37 dB at 226 MHz, with increasing attenuation at higher frequencies. Diode CR1 protects the RF amplifier by limiting excessive RF levels.

The output of the filter is matched to the base of RF amplifier Q21, which provides 18 dB of gain and a noise figure of 2 dB. Operating voltage is obtained from the 5R source, which is turned off during transmit to reduce dissipation in Q21. Current mirror Q22 maintains the operating current of Q21

constant at 6.2 mA regardless of device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the interstage filter, a fixed-tuned 3-pole series-coupled resonator design having a 3 dB bandwidth of 54 MHz and insertion loss of 1.8 dB. This filter has an image rejection of 40 dB at 226 MHz, with increasing attenuation at higher frequencies.

The output of the interstage filter is connected to the passive double-balanced mixer consisting of components T41, T42, and CR41. This mixer has a conversion loss of 7 dB. High-side injection from the frequency synthesizer is filtered by L40-L41 and C40-C44 to remove second harmonic energy that may degrade half-IF spurious rejection performance. The injection filter has a 3 dB bandwidth of 52 MHz and an insertion loss of 1.5 dB. The filtered injection signal is applied to T42 at a level of +6 dBm.

The mixer output is applied to a diplexer network (L51-L52, C51, R51) which matches the 44.85 MHz IF signal to crystal filter FL51, and terminates the mixer into 50Ω at all other frequencies

4.2.2 Receiver Back-End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL51, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of + 6.7 kHz, a maximum 20 dB bandwidth of ±12.5 kHz, and a maximum insertion loss of 3.5 dB. The output is matched to IF amplifier stage Q51 by L53 and C93. Q51 provides 16 dB of gain and a noise figure of 1.8 dB. The dc operating current is 1 mA. The output of Q51 is applied to the input of the receiver IFIC U51. Diode CR51 limits the maximum RF level applied to the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency, 44.395 MHz, is determined by Y51. The second mixer converts the 44.85 MHz high IF frequency to 455 kHz.

Additional IF selectivity is provided by two ceramic filters, FL52 (between the second mixer and IF amp) and FL53 or FL54 (between the IF amp and the limiter input). The wider filter FL53 is used for 20/25 kHz channel spacing, and the narrower filter FL54 is used for 12.5 kHz channels. When the BW_SEL line is high, the two upper diodes in packages D51 and D52 are forward biased, selecting FL53 for 20/25 kHz channels. When the BW_SEL line is low, the two lower diodes in packages D51 and D52 are forward biased, selecting FL54 for 12.5 kHz channels.

	FL52	FL53	FL54
Number of Elements:	4	6	6
Insertion Loss:	4 dB	4 dB	4 dB
6 dB Bandwidth:	15 kHz	15 kHz	9 kHz
50 dB Bandwidth:	30 kHz	30 kHz	22 kHz
Stopband Rejection:	27 dB	47 dB	47 dB

Ceramic resonator Y70 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q70 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering the distortion of the recovered audio signal. The recovered audio level at the DEMOD output is 120 mV rms (25 kHz channel, 3 kHz deviation) or 60 mV rms (12.5 kHz channel, 1.5 kHz deviation). An additional RSSI output provides a DC voltage level that is proportional to RF signal level. This voltage is measured by an A/D converter contained in the microprocessor (PE4_AN4, U401 pin 63).

4.3 VHF Transmitter

The VHF transmitter covers the range of 136-162 MHz. Depending on model, the output power of the transmitter is either switchable on a per-channel basis between high power (5 watts) and low power (1 watt), or is factory preset to 2 watts. The transmitter is divided into four major blocks as shown in Figure 4-2.

- Power Amplifier
- Harmonic Filter
- Antenna Matching Network
- Power Control

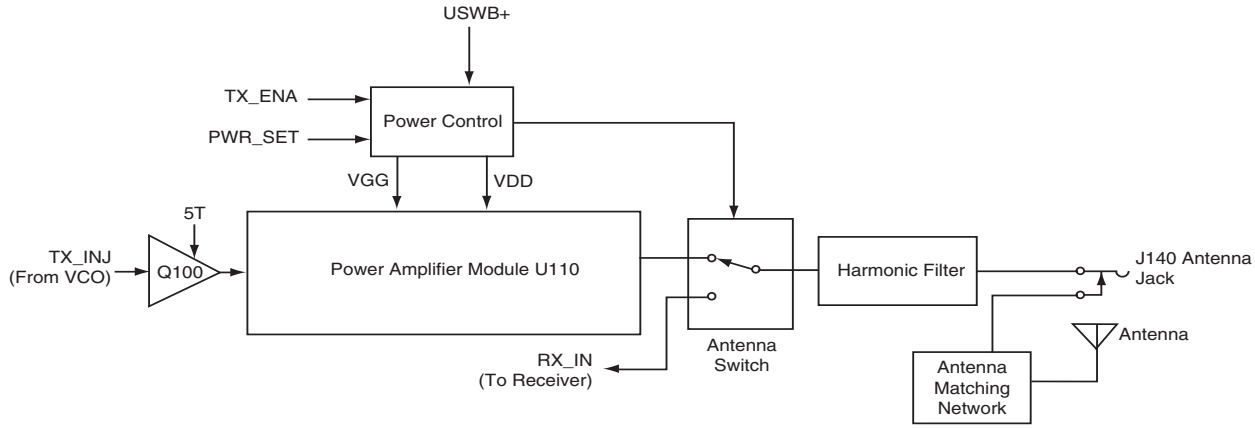

Figure 4-2. VHF Transmitter Block Diagram

4.3.1 Transmit Power Amplifier

The transmitter power amplifier has three stages of amplification. The first stage, Q100, operates in Class AB from the 5T source. It provides 13 dB of gain and an output of 20 mW. The current drain is typically 25mA. Components C105-C107 and L103 match the output of Q100 to the 50Ω input of the module U110.

U110 is a two stage Silicon MOS FET power amplifier module. Drain voltage is obtained from UNSW B+ after being routed through current-sense resistor R150 in the power control circuit. The output power of the module is controlled by varying the DC gate bias on U110 pin 2 (VGG).

4.3.2 Antenna Switch

The antenna switch consists of two pin diodes, D120 and D121. In the receive mode, both diodes are off. Signals applied at the antenna or at jack J140 are routed, via the harmonic filter, through network C122-C124 and L121, to the receiver input. In the transmit mode, Q170 is on and TXB+ is present, forward-biasing both diodes into conduction. The diode current is 50 mA, set by R120-R122. The transmitter RF from U110 is routed through D120, and via the harmonic filter to the antenna jack. D121 conducts, shunting RF power and preventing it from reaching the receiver. L121 is selected to appear as a 1/4 wave at VHF, so that the low impedance of D121 appears as a high impedance at the junction of D120 and the harmonic filter input. This provides a high series impedance and low shunt impedance divider between the power amplifier output and receiver input.

4.3.3 Harmonic Filter

The harmonic filter consists of components C130-C136 and L130-L132. The harmonic filter is a seven-pole elliptical low-pass configuration, optimized for low insertion loss, with a 3 dB frequency of approximately 180 MHz and typically less than 0.8 dB insertion loss in the passband.

4.3.4 Antenna Matching Network

The harmonic filter presents a 50 Ω impedance to antenna jack J140. A matching network, made up of C140-C141 and L140, is used to match the antenna impedance to the harmonic filter. This optimizes the performance of the transmitter and receiver into the impedance presented by the antenna, significantly improving the antenna's efficiency.

4.3.5 Power Control

The power control circuit is a dc-coupled amplifier whose output is the dc gate bias voltage (VGG) applied to the two stages of the RF power amplifier U110.

The output power of the transmitter is adjusted by varying the setting of the power-set DAC contained in the ASFICcmp IC (DACG, U451 pin 6). This PWR_SET voltage is applied to U150 pin 3.

Stage U150-2 compares the voltage drop across current sense resistor R150 to the voltage drop across resistor R151 caused by current flow through Q150, and adjusts its output (pin 7) to maintain equal voltages at pins 5 and 6. Thus the current flow through Q150, and hence its emitter voltage, is proportional to the current drawn by stage U110, which is in turn proportional to the transmitter output power. The emitter voltage of Q150 is applied to U150 pin 2, where it is compared to the power set voltage PWR_SET at pin 3.

The output of U150 pin 1 is divided by R110 and R111 and applied as a gate voltage to the power amplifier U110. By varying this gate voltage as needed to keep the voltages at U150 pins 2 and 3 equal, power is maintained at the desired setting. Excessive final current, for example due to antenna mismatch, causes a lowering of the voltage at U150 pin 6, an increased voltage at pin 2, and a lowering of the voltage at pin 1 and of the gate voltage VGG. This prevents damage to the final stage due to excessive current.

4.4 VHF Frequency Generation Circuitry

The frequency generation system, shown in Figure 4-3, is composed of two circuit blocks, the Fractional-N synthesizer IC U201, the VCO/Buffer IC U251, and associated circuitry. Figure 4-4 shows the peripheral interconnect and support circuitry used in the synthesizer block, and Figure 4-5 details the internal circuitry of the VCOBIC and its interconnections to the surrounding components. Refer to the schematic to identify reference designators.

The Fractional-N synthesizer is powered by regulated 5 V and 3 V provided by U310 and U330 respectively. 5 V is applied to U201 pins 13 and 30, and 3 V is applied to pins 5, 20, 34 and 36. The synthesizer in turn generates a super-filtered 4.5 V supply (VSF, from pin 28) to power U251. In addition to the VCO, the synthesizer also interfaces with the logic and ASFICcmp circuits. Programming for the synthesizer is accomplished through the microprocessor SPI_DATA_OUT, SPI_CLK, and SYNTH_CS (chip select) lines (U409 pins 100, 1 and 47 respectively). A logic high (3 V) from U201 pin 4 indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFICcmp (U451 pin 40) is applied to U201 pin 10 (MOD_IN). An electronic attenuator in the ASFICcmp adjusts overall transmitter deviation by varying the audio level applied to the synthesizer IC. Internally the audio is digitized by the Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio is also routed through an internal attenuator for the purpose of balancing the low port and high port modulation and reducing the deviation by 6 dB for 12.5 kHz channels, and is available at U201 pin 41 (VCO_MOD). This audio signal is routed to the VCO's modulator.

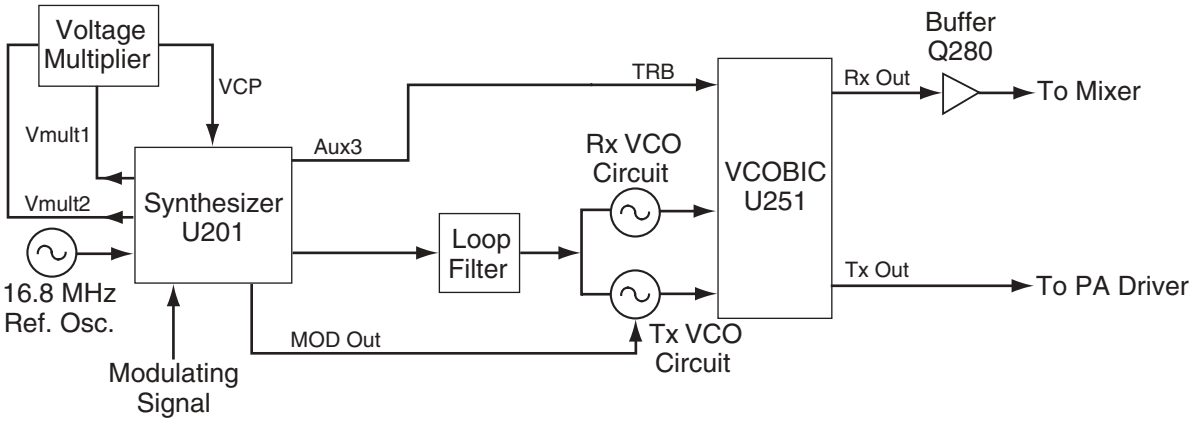

Figure 4-3. VHF Frequency Generation Unit Block Diagram

4.4.1 Fractional-N Synthesizer

The Fractional-N synthesizer, shown in Figure 4-4, uses a 16.8 MHz crystal (Y201) to provide the reference frequency for the system. External components C201-C203, R202 and D201 are also part of the temperature-compensated oscillator circuit. The dc voltage applied to varactor D201 from U201 pin 25 is determined by a temperature-compensation algorithm within U201, and is specific to each crystal Y201, based on a unique code assigned to the crystal that identifies its temperature characteristics. Stability is better than 2.5 ppm over temperatures of -30 to 60 °C. Software-programmable electronic frequency adjustment is achieved by an internal DAC which provides a frequency adjustment voltage from U201 pin 25 to varactor D201.

The synthesizer IC U201 further divides the 16.8 MHz signal to 2.1 MHz, 2.225 MHz, or 2.4 MHz for use as reference frequencies. It also provides a buffered 16.8 MHz signal at U201 pin 19 for use by the ASFICcmp.

To achieve fast locking of the synthesizer, an internal adapt charge pump provides higher current at U201 pin 45 to quickly force the synthesizer within lock range. The required frequency is then locked by the normal mode charge pump at pin 43. A loop filter (C243-C245 and R243-R245) removes noise and spurs from the steering voltage applied to the VCO varactors, with additional filtering located in the VCO circuit.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C221-C224 and D220-D221. Two 3 V square waves from U201 pins 14-15 provide the drive signals for the voltage multiplier, which generates 12.1 V at U201 pin 47. This voltage is filtered by C225-C228.

One of the auxiliary outputs of the synthesizer IC (AUX3, U201 pin 2) provides the TRB signal which determines the operating mode of the VCO, either receive or transmit.

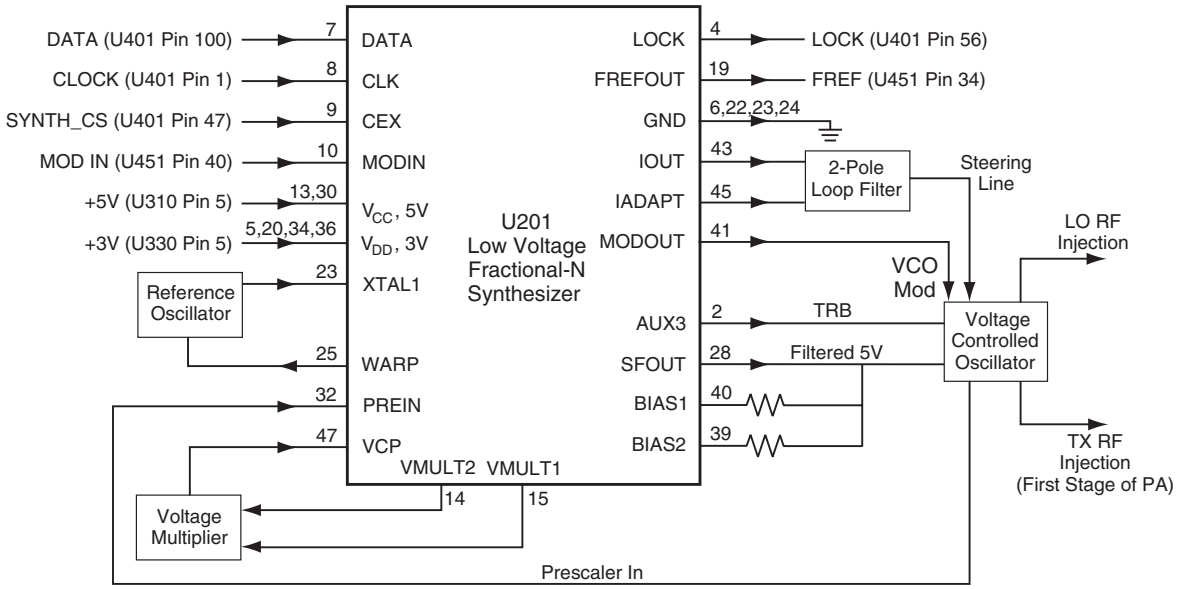

Figure 4-4. VHF Synthesizer Block Diagram

4.4.2 Voltage Controlled Oscillator (VCO)

The VCOBIC (U251), shown in Figure 4-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U251 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U251 pin 12 through a low pass filter, to the prescaler input of the synthesizer IC (U201 pin 32). After frequency comparison in the synthesizer, a resultant DC control voltage is used to steer the VCO frequency. When the PLL is locked on frequency, this voltage can vary between 3 V and 9 V. L251 and C251 further attenuate noise and spurs on the steering line voltage.

In the receive mode, the TRB line (U251 pin 19) is low. This activates the receive VCO and the receive buffer of U251, which operate within the range of 180.85 to 206.85 MHz. The VCO frequency is determined by tank inductor L254, C253-C257, and varactor D251. The buffered RF signal at U251 pin 8 is further amplified by Q280 and applied as RX_INJ to the low-pass injection filter in the receiver front end circuit.

In the transmit mode, U251-19 is driven high by U201 pin 2, enabling the transmit VCO and buffer. The 136-162 MHz RF signal from U251 pin 10 is applied as TX_INJ to the input of the transmitter circuit via matching network C290-C291 and L291. TX VCO frequency is determined by L264, C263-

C267, and varactor D261. High-port audio modulation from the synthesizer IC is applied as VCO_MOD to varactor D262 which modulates the transmit VCO.

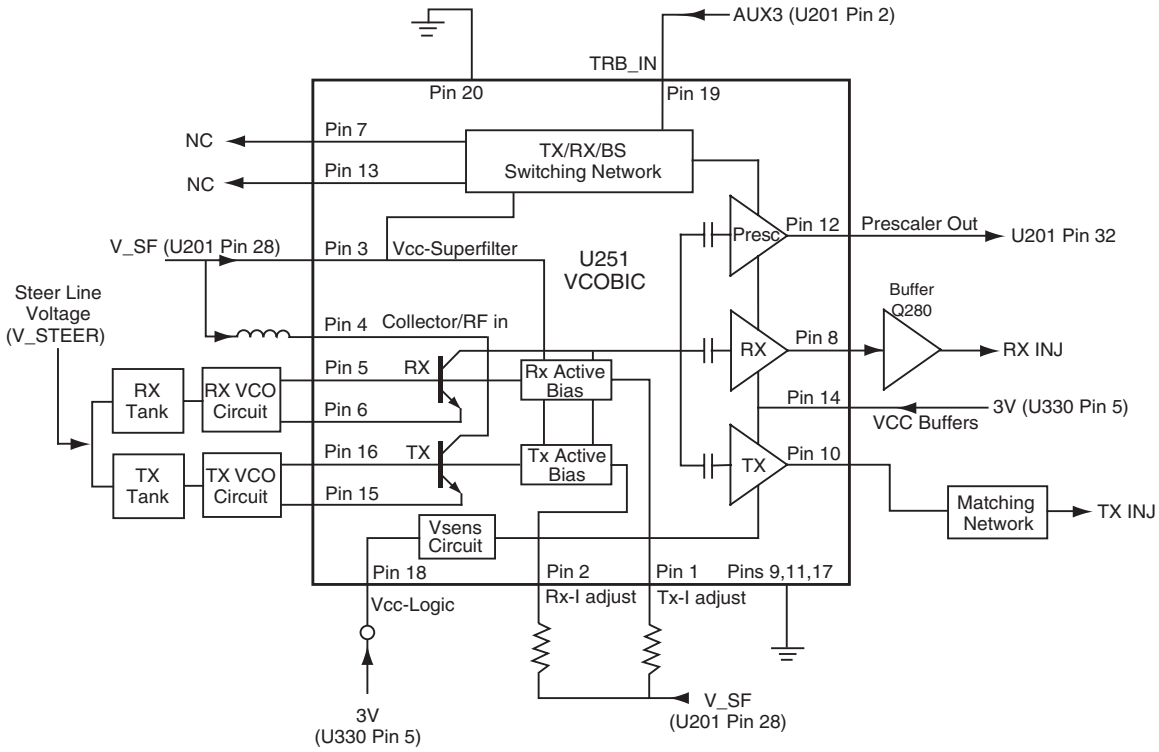

Figure 4-5. VHF VCO Block Diagram

4.5 Keypad

The keypad block diagram is shown in Figure 4-6. Pressing a key creates two distinct voltages KEYPAD_ROW and KEYPAD_COL. These voltages are sent directly to the radio's microprocessor on the main board. The microprocessor then interprets the voltage for KEYPAD_ROW and KEYPAD_COL for each key press.

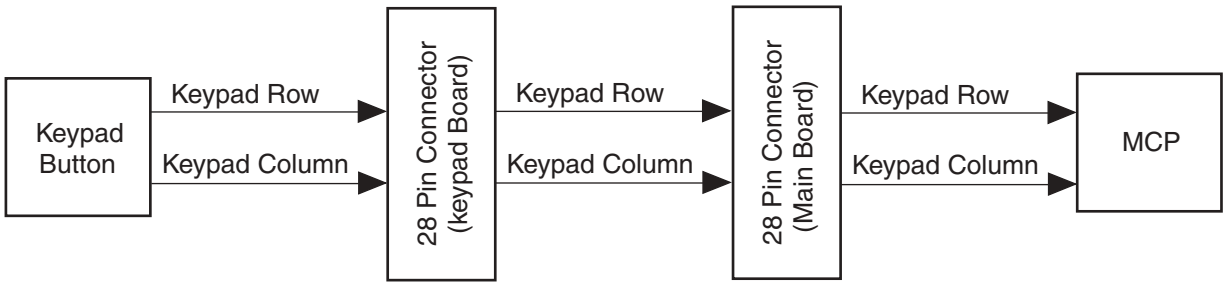

Figure 4-6. Keypad Block Diagram

Notes:

Chapter 5 146-174 MHz VHF Theory Of Operation

5.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Chapter 7 of this manual.

5.2 VHF Receiver

The VHF receiver covers the range of 146-174 MHz and provides switchable IF bandwidth for use with 12.5 kHz or 20/25 kHz channel spacing systems. The receiver is divided into two major blocks as shown in Figure 5-1.

- Front End
- Back End

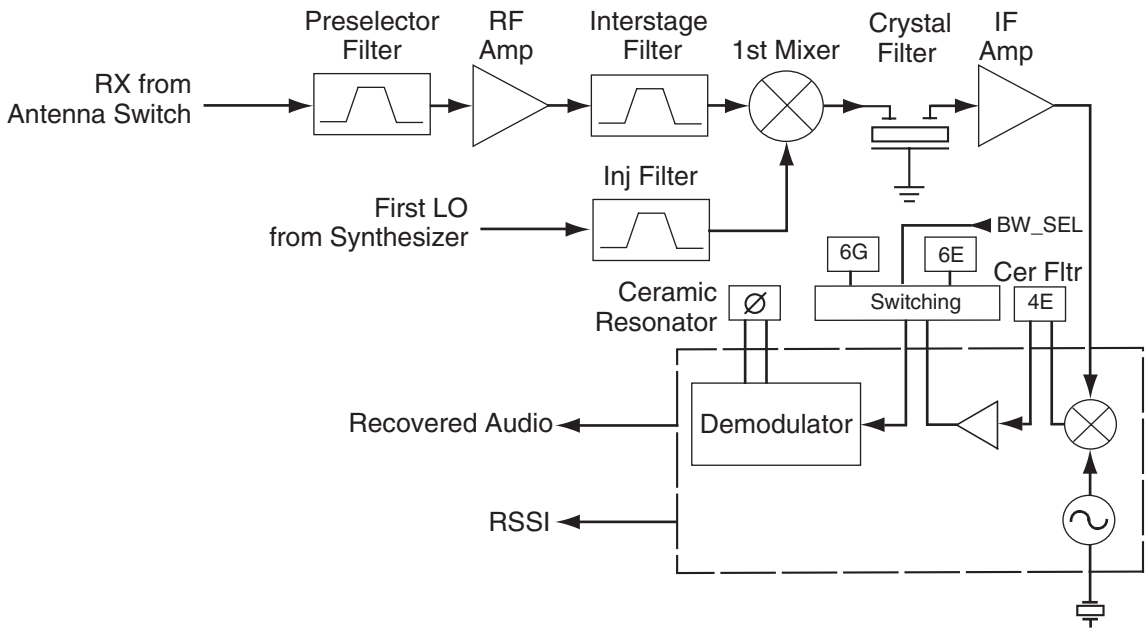

Figure 5-1. VHF Receiver Block Diagram

5.2.1 Receiver Front-End

Incoming RF signals from the antenna are first routed through the harmonic filter and antenna switch, part of the transmitter circuitry, before being applied to the receiver front end. The receiver front end consists of a preselector filter, RF amplifier, an interstage filter, and a double-balanced first mixer.

The preselector filter is a fixed-tuned 4-pole design using discrete elements (L1-L4 and C1-C9) in a series/shunt resonator configuration. It has a 3 dB bandwidth of 44 MHz, an insertion loss of 2 dB and image attenuation of 40 dB at 235 MHz, with increasing attenuation at higher frequencies. Diode CR1 protects the RF amplifier by limiting excessive RF levels.

The output of the filter is matched to the base of RF amplifier Q21, which provides 18 dB of gain and a noise figure of 2 dB. Operating voltage is obtained from the 5R source, which is turned off during transmit to reduce dissipation in Q21. Current mirror Q22 maintains the operating current of Q21

constant at 6.2 mA regardless of device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the interstage filter, a fixed-tuned 3-pole series-coupled resonator design having a 3 dB bandwidth of 58 MHz and insertion loss of 1.8 dB. This filter has an image rejection of 42 dB at 235 MHz, with increasing attenuation at higher frequencies.

The output of the interstage filter is connected to the passive double-balanced mixer consisting of components T41, T42, and CR41. This mixer has a conversion loss of 7 dB. High-side injection from the frequency synthesizer is filtered by L40-L41 and C40-C44 to remove second harmonic energy that may degrade half-IF spurious rejection performance. The injection filter has a 3 dB bandwidth of 52 MHz and an insertion loss of 1.5 dB. The filtered injection signal is applied to T42 at a level of +6 dBm.

The mixer output is applied to a diplexer network (L51-L52, C51, R51) which matches the 44.85 MHz IF signal to crystal filter FL51, and terminates the mixer into 50Ω at all other frequencies

5.2.2 Receiver Back-End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL51, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of + 6.7 kHz, a maximum 20 dB bandwidth of ±12.5 kHz, and a maximum insertion loss of 3.5 dB. The output is matched to IF amplifier stage Q51 by L53 and C93. Q51 provides 16 dB of gain and a noise figure of 1.8 dB. The dc operating current is 1 mA. The output of Q51 is applied to the input of the receiver IFIC U51. Diode CR51 limits the maximum RF level applied to the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency, 44.395 MHz, is determined by Y51. The second mixer converts the 44.85 MHz high IF frequency to 455 kHz.

Additional IF selectivity is provided by two ceramic filters, FL52 (between the second mixer and IF amp) and FL53 or FL54 (between the IF amp and the limiter input). The wider filter FL53 is used for 20/25 kHz channel spacing, and the narrower filter FL54 is used for 12.5 kHz channels. When the BW_SEL line is high, the two upper diodes in packages D51 and D52 are forward biased, selecting FL53 for 20/25 kHz channels. When the BW_SEL line is low, the two lower diodes in packages D51 and D52 are forward biased, selecting FL54 for 12.5 kHz channels.

	FL52	FL53	FL54
Number of Elements:	4	6	6
Insertion Loss:	4 dB	4 dB	4 dB
6 dB Bandwidth:	15 kHz	15 kHz	9 kHz
50 dB Bandwidth:	30 kHz	30 kHz	22 kHz
Stopband Rejection:	27 dB	47 dB	47 dB

Ceramic resonator Y70 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q70 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering the distortion of the recovered audio signal. The recovered audio level at the DEMOD output is 120 mV rms (25 kHz channel, 3 kHz deviation) or 60 mV rms (12.5 kHz channel, 1.5 kHz deviation). An additional RSSI output provides a DC voltage level that is proportional to RF signal level. This voltage is measured by an A/D converter contained in the microprocessor (PE4_AN4, U401 pin 63).

5.3 VHF Transmitter

The VHF transmitter covers the range of 146-174 MHz. Depending on model, the output power of the transmitter is either switchable on a per-channel basis between high power (5 watts) and low power (1 watt). The transmitter is divided into four major blocks as shown in Figure 5-2.

- Power Amplifier
- Harmonic Filter
- Antenna Matching Network
- Power Control

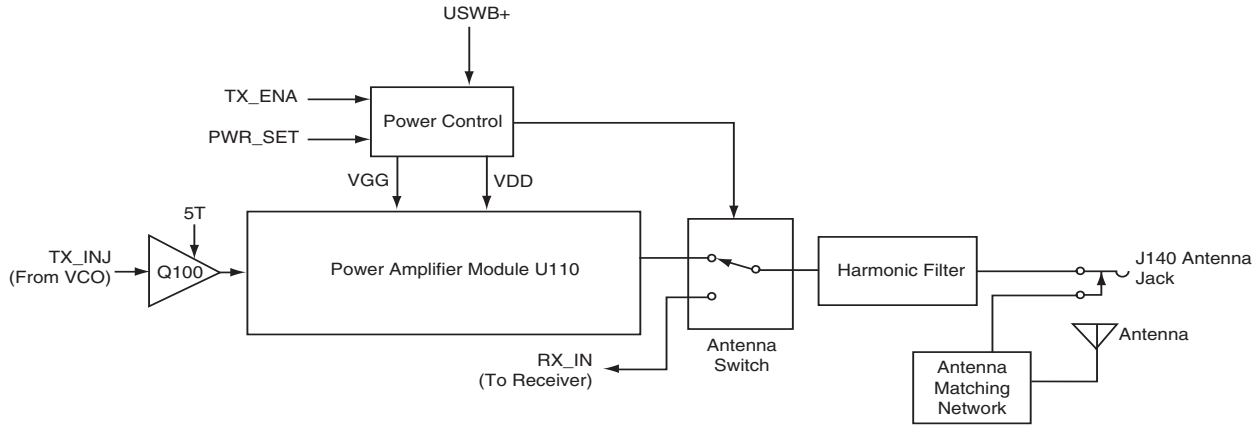

Figure 5-2. VHF Transmitter Block Diagram

5.3.1 Transmit Power Amplifier

The transmitter power amplifier has three stages of amplification. The first stage, Q100, operates in Class AB from the 5T source. It provides 13 dB of gain and an output of 20 mW. The current drain is typically 25mA. Components C105-C107 and L103 match the output of Q100 to the 50Ω input of the module U110.

U110 is a two stage Silicon MOS FET power amplifier module. Drain voltage is obtained from UNSW B+ after being routed through current-sense resistor R150 in the power control circuit. The output power of the module is controlled by varying the DC gate bias on U110 pin 2 (VGG).

5.3.2 Antenna Switch

The antenna switch consists of two pin diodes, D120 and D121. In the receive mode, both diodes are off. Signals applied at the antenna or at jack J140 are routed, via the harmonic filter, through network C122-C124 and L121, to the receiver input. In the transmit mode, Q170 is on and TXB+ is present, forward-biasing both diodes into conduction. The diode current is 50 mA, set by R120-R122. The transmitter RF from U110 is routed through D120, and via the harmonic filter to the antenna jack. D121 conducts, shunting RF power and preventing it from reaching the receiver. L121 is selected to appear as a 1/4 wave at VHF, so that the low impedance of D121 appears as a high impedance at the junction of D120 and the harmonic filter input. This provides a high series impedance and low shunt impedance divider between the power amplifier output and receiver input.

5.3.3 Harmonic Filter

The harmonic filter consists of components C130-C136 and L130-L132. The harmonic filter is a seven-pole elliptical low-pass configuration, optimized for low insertion loss, with a 3 dB frequency of approximately 210 MHz and typically less than 0.8 dB insertion loss in the passband.

5.3.4 Antenna Matching Network

The harmonic filter presents a 50 Ω impedance to antenna jack J140. A matching network, made up of C140-C141 and L140, is used to match the antenna impedance to the harmonic filter. This optimizes the performance of the transmitter and receiver into the impedance presented by the antenna, significantly improving the antenna's efficiency.

5.3.5 Power Control

The power control circuit is a dc-coupled amplifier whose output is the dc gate bias voltage (VGG) applied to the two stages of the RF power amplifier U110.

The output power of the transmitter is adjusted by varying the setting of the power-set DAC contained in the ASFICcmp IC (DACG, U451 pin 6). This PWR_SET voltage is applied to U150 pin 3.

Stage U150-2 compares the voltage drop across current sense resistor R150 to the voltage drop across resistor R151 caused by current flow through Q150, and adjusts its output (pin 7) to maintain equal voltages at pins 5 and 6. Thus the current flow through Q150, and hence its emitter voltage, is proportional to the current drawn by stage U110, which is in turn proportional to the transmitter output power. The emitter voltage of Q150 is applied to U150 pin 2, where it is compared to the power set voltage PWR_SET at pin 3.

The output of U150 pin 1 is divided by R110 and R111 and applied as a gate voltage to the power amplifier U110. By varying this gate voltage as needed to keep the voltages at U150 pins 2 and 3 equal, power is maintained at the desired setting. Excessive final current, for example due to antenna mismatch, causes a lowering of the voltage at U150 pin 6, an increased voltage at pin 2, and a lowering of the voltage at pin 1 and of the gate voltage VGG. This prevents damage to the final stage due to excessive current.

5.4 VHF Frequency Generation Circuitry

The frequency generation system, shown in Figure 5-3, is composed of two circuit blocks, the Fractional-N synthesizer IC U201, the VCO/Buffer IC U251, and associated circuitry. Figure 5-4 shows the peripheral interconnect and support circuitry used in the synthesizer block, and Figure 5-5 details the internal circuitry of the VCOBIC and its interconnections to the surrounding components. Refer to the schematic to identify reference designators.

The Fractional-N synthesizer is powered by regulated 5 V and 3 V provided by U310 and U330 respectively. 5 V is applied to U201 pins 13 and 30, and 3 V is applied to pins 5, 20, 34 and 36. The synthesizer in turn generates a super-filtered 4.5 V supply (VSF, from pin 28) to power U251. In addition to the VCO, the synthesizer also interfaces with the logic and ASFICcmp circuits. Programming for the synthesizer is accomplished through the microprocessor SPI_DATA_OUT, SPI_CLK, and SYNTH_CS (chip select) lines (U409 pins 100, 1 and 47 respectively). A logic high (3 V) from U201 pin 4 indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFICcmp (U451 pin 40) is applied to U201 pin 10 (MOD_IN). An electronic attenuator in the ASFICcmp adjusts overall transmitter deviation by varying the audio level applied to the synthesizer IC. Internally the audio is digitized by the Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio is also routed through an internal attenuator for the purpose of balancing the low port and high port modulation and reducing the deviation by 6 dB for 12.5 kHz channels, and is available at U201 pin 41 (VCO_MOD). This audio signal is routed to the VCO's modulator.

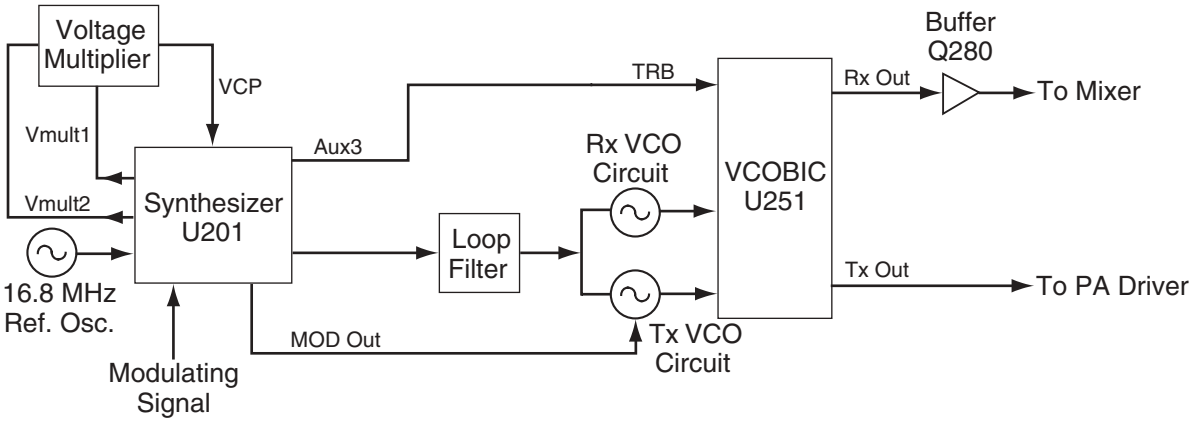

Figure 5-3. VHF Frequency Generation Unit Block Diagram

5.4.1 Fractional-N Synthesizer

The Fractional-N synthesizer, shown in Figure 5-4, uses a 16.8 MHz crystal (Y201) to provide the reference frequency for the system. External components C201-C203, R202 and D201 are also part of the temperature-compensated oscillator circuit. The dc voltage applied to varactor D201 from U201 pin 25 is determined by a temperature-compensation algorithm within U201, and is specific to each crystal Y201, based on a unique code assigned to the crystal that identifies its temperature characteristics. Stability is better than 2.5 ppm over temperatures of -30 to 60 °C. Software-programmable electronic frequency adjustment is achieved by an internal DAC which provides a frequency adjustment voltage from U201 pin 25 to varactor D201.

The synthesizer IC U201 further divides the 16.8 MHz signal to 2.1 MHz, 2.225 MHz, or 2.4 MHz for use as reference frequencies. It also provides a buffered 16.8 MHz signal at U201 pin 19 for use by the ASFICcmp.

To achieve fast locking of the synthesizer, an internal adapt charge pump provides higher current at U201 pin 45 to quickly force the synthesizer within lock range. The required frequency is then locked by the normal mode charge pump at pin 43. A loop filter (C243-C245 and R243-R245) removes noise and spurs from the steering voltage applied to the VCO varactors, with additional filtering located in the VCO circuit.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C221-C224 and D220-D221. Two 3 V square waves from U201 pins 14-15 provide the drive signals for the voltage multiplier, which generates 12.1 V at U201 pin 47. This voltage is filtered by C225-C228.

One of the auxiliary outputs of the synthesizer IC (AUX3, U201 pin 2) provides the TRB signal which determines the operating mode of the VCO, either receive or transmit.

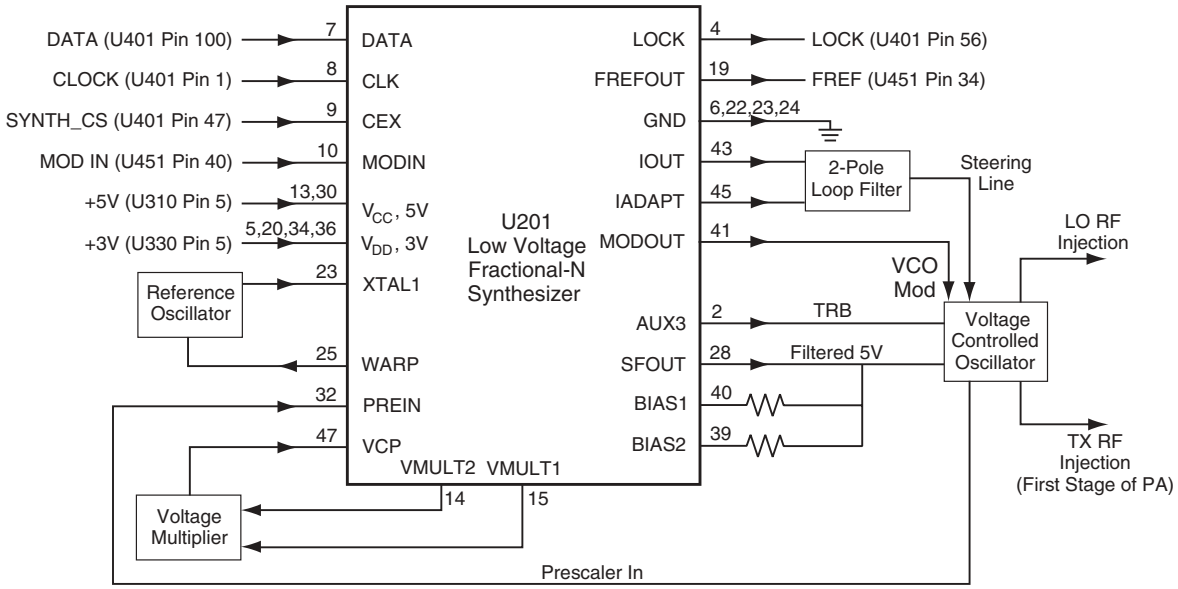

Figure 5-4. VHF Synthesizer Block Diagram

5.4.2 Voltage Controlled Oscillator (VCO)

The VCOBIC (U251), shown in Figure 5-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U251 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U251 pin 12 through a low pass filter, to the prescaler input of the synthesizer IC (U201 pin 32). After frequency comparison in the synthesizer, a resultant DC control voltage is used to steer the VCO frequency. When the PLL is locked on frequency, this voltage can vary between 3 V and 9 V. L251 and C251 further attenuate noise and spurs on the steering line voltage.

In the receive mode, the TRB line (U251 pin 19) is low. This activates the receive VCO and the receive buffer of U251, which operate within the range of 190.85 to 218.85 MHz. The VCO frequency is determined by tank inductor L254, C253-C257, and varactor D251. The buffered RF signal at U251 pin 8 is further amplified by Q280 and applied as RX_INJ to the low-pass injection filter in the receiver front end circuit.

In the transmit mode, U251-19 is driven high by U201 pin 2, enabling the transmit VCO and buffer. The 146-174 MHz RF signal from U251 pin 10 is applied as TX_INJ to the input of the transmitter circuit via matching network C290-C291 and L291. TX VCO frequency is determined by L264, C263-

C267, and varactor D261. High-port audio modulation from the synthesizer IC is applied as VCO_MOD to varactor D262 which modulates the transmit VCO.

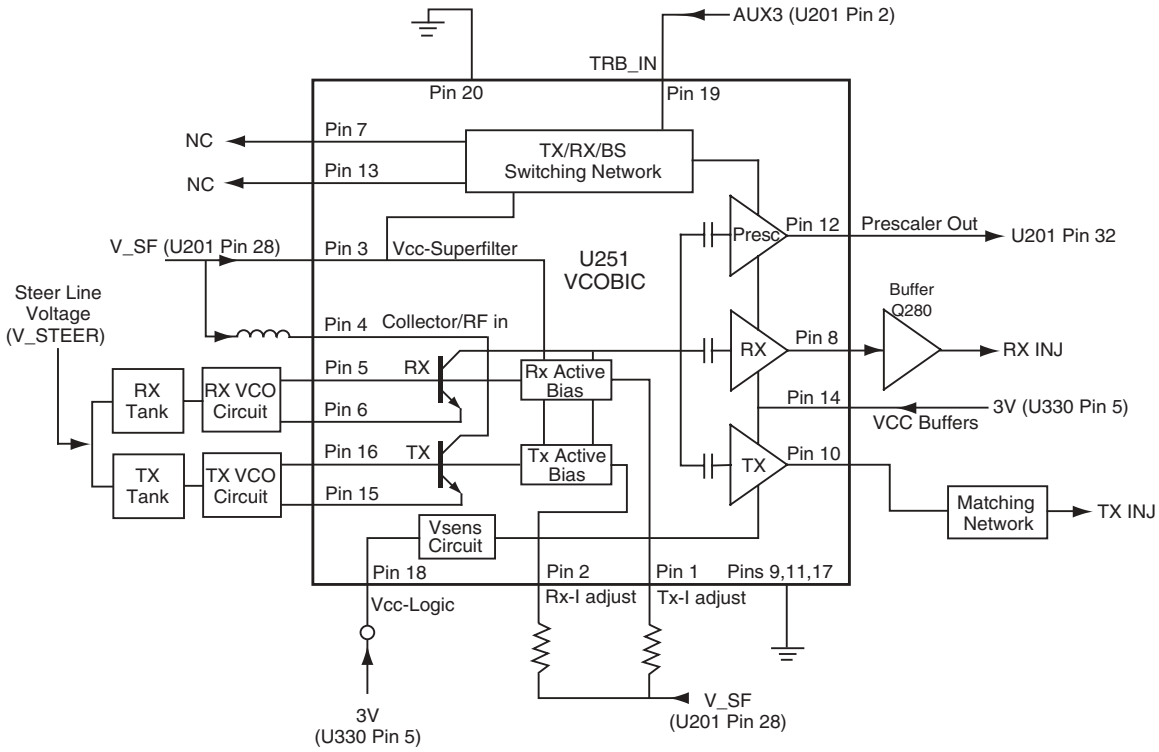

Figure 5-5. VHF VCO Block Diagram

5.5 Keypad

The keypad block diagram is shown in Figure 5-6. Pressing a key creates two distinct voltages KEYPAD_ROW and KEYPAD_COL. These voltages are sent directly to the radio's microprocessor on the main board. The microprocessor then interprets the voltage for KEYPAD_ROW and KEYPAD_COL for each key press.

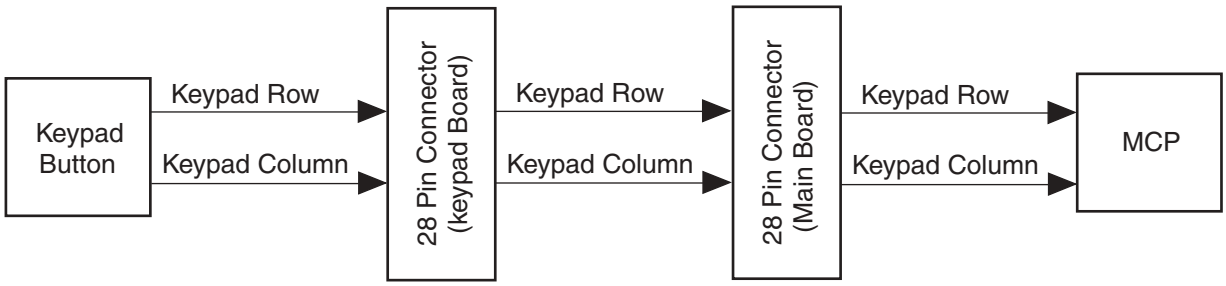

Figure 5-6. Keypad Block Diagram

Notes:

Chapter 6 VHF Troubleshooting Tables

6.1 Troubleshooting Table for Receiver

Table 6-1. Troubleshooting Table for Receiver

Symptom	Possible Causes	Procedure	Corrective Action
Radio Dead (no turn-on beep, no LED indication)	1. Battery dead or defective.	Substitute known good battery or battery eliminator.	Charge or replace battery.
	2. Defective battery contacts.	Inspect battery contacts for corrosion or bent terminals.	Clean/repair/replace J301.
	3. Blown fuse	Check voltage on each side of fuse. If blown, 0 VDC after fuse.	Check for short on output, check D301, VR301, troubleshoot/repair as needed, replace fuse.
	4. DC switching fault	Verify battery voltage present at S444 pin 5 when radio is on. Verify Q494-1 is at least 1 V dc, Q494-6 is ~0.1 V dc, Q493-3 is at Vbatt.	Check/replace on-off-volume control S444. Troubleshoot/replace Q493/4.
	5. Microprocessor not starting up.	Verify clock input to U401-90 (EXTAL) is 7.3975 MHz using high impedance probe. If clock is 3.8 MHz, check for shorts on U401 pins. Connect RIB to verify communication via CPS. Verify U401-94 (RESET) is high.	Verify 16.8 MHz signal at U451-34. If OK, troubleshoot/replace U451. If not present, troubleshoot U201 Synthesizer. Reprogram/reflash as needed. If RESET is Low, troubleshoot regulator U320. Check for shorts at U401 pins. Replace U401. Reprogram as needed.
	6. Regulator fault	Verify U310-5 is 5 V dc, U320-5 is 3.3 V dc, U330-5 is 3 V dc.	Check for shorts on outputs, troubleshoot/repair as needed, replace faulty regulator.

Table 6-1. Troubleshooting Table for Receiver (Continued)

Symptom	Possible Causes	Procedure	Corrective Action
No Audio	1. Synthesizer out of lock	Verify U201-4 is at 3 V dc.	Troubleshoot synthesizer/VCO circuits.
	2. Defective IFIC	Verify audio is present at U51-8.	Check Q70, Y70, U51.
	3. RX audio buffer fault	Verify audio is present at U451-2.	Check U510 and associated parts.
	4. ASFIC fault	Verify audio is present at U451-41. Verify U451-14 is high.	Check squelch setting, PL/DPL programming. Troubleshoot/ replace U451.
	5. Audio PA fault	Verify U490-1 is <0.2 V dc. Verify audio is present at U490-5 and 8.	Check Q490. Check/replace U490.
	6. Defective speaker	Verify audio is present at speaker terminals.	If not, check continuity of J471-2 and 3. Check J491. If yes, replace speaker.
No Receive (squelch noise present)	1. No first injection	Check that RF level at T42-6 is approx +6 dBm. Check that RF level at U251-8 is at least -8 dBm.	Check injection filter C40-44, L40-41. If yes, check Q280 and associated parts. If no, check U251 and components on pins 5 and 6.
	2. No 5R source.	Verify U401-49 is high in RX. Verify Q311 gate is 0 V dc in RX Verify Q311 drain is 5 V dc in RX.	Check/replace U401 Check/replace Q313. Check for shorts, check/replace Q311.
	3. Harmonic filter or antenna switch fault	Apply on-channel 100 mV RF signal at antenna port. Verify RF level at jct. C1/C2 per schematic.	Check TX harmonic filter, D120-121. Should be 0 V dc on D120-121.
	4. Back end fault	Apply on-channel 100 mV RF signal at antenna port. Measure RF levels from FL51 through U51.	Check components prior to loss-of-signal point.
	5. No second injection	Measure RF level at U51-3, verify approx. 280 mV rms.	If dc voltages at U51-3 and 4 are OK, check Y51 and associated parts. If not replace U51.

6.2 Troubleshooting Table for Synthesizer

Table 6-2. Troubleshooting Table for Synthesizer

Symptom	Possible Causes	Procedure	Corrective Action
Synthesizer Out of Lock (RX mode only)	1. VCO fault	Verify oscillator is working, check RF level at U251-10 per schematic. Check dc voltages at U251 pin 2 through 6 and 10 per Table 6-4. Verify steering line voltage is between ~3 V and 10 V.	Check VCO tank components connected to U251-5 and 6. Check for shorts/opens, replace U251. Check D251 and associated components.
	2. Synthesizer fault	Verify TRB line (from U201-2 to U251-19) is low in RX mode	Check for shorts, check U201 voltages per Table 6-4, replace U201 if incorrect.
	3. Programming fault	Verify RX channel programming is correct.	Re-program if necessary.
Synthesizer Out of Lock (TX mode only)	1. VCO fault	Verify oscillator is working, check RF level at U251-10 per schematic. Check dc voltages at U251 pins 1,3,4,10,15,16 per Table 6-4. Verify steering line voltage is between ~3 V and 10 V.	Check VCO tank components connected to U251-15 and 16. Check for shorts/opens, replace U251. Check D261 and associated components.
	2. Synthesizer fault	Verify TRB line (U201-2 to U251-19) is high (3 V) in TX mode	Check for shorts, check U201 voltages per Table 6-4, replace U201 if incorrect.
	3. Programming fault	Verify TX channel programming is correct.	Re-program if necessary.
Synthesizer Out of Lock (RX and TX modes)	1. VCO fault	Check that RF level at U251-12 is at least 150 mV (VHF) or -12 to -20 dBm (UHF)	If low/missing, check L276, C276-7, R276.
	2. Synthesizer fault	Check that RF level at U201-32 is at least 150 mV (VHF) or -12 to -20 dBm (UHF). Verify steering line voltage is between ~3 V and 10 V.	If correct, check/replace U201. If incorrect, check R248 and C241. Check loop filter components R243-5 and C243-5.
	3. DC voltage fault	Verify 4.5 V dc at U201-28. Verify 12.1 V dc at U201-47	Check C231-233, etc., for shorts. If OK check/replace U201. Check for 3 V 1.05 MHz sq waves at U201-14 and 15. Check C218-228, D220-221.
	4. Programming fault	Verify channel programming is correct.	Re-program if necessary.

6.3 Troubleshooting Table for Transmitter

Table 6-3. Troubleshooting Table for Transmitter

Symptom	Possible Causes	Procedure	Corrective Action
No Transmit (no TX LED indication)	1. PTT switch defective.	Verify U401-71 goes low when PTT is pressed.	Replace PTT switch S441.
	2. EXT MIC PTT fault	Verify U401-72 goes low when J471-4 is grounded.	Check/replace Q470, L471 etc.
No Transmit (TX LED indication OK)	1. Synthesizer out of lock	Refer to Table 6-2.	Refer to Table 6-2.
	2. No TX_ENABLE	Verify U401-50 is high when pin 71 or 72 is low.	Check/replace U401.
	3. TX DC switch fault	Verify Q171-C is 0 V in TX. Verify Q170-C is at Vbatt in TX.	Replace Q171. Check for shorts, replace Q170.
	4. Power control fault	Check Q150 and U150 dc voltages per schematic and Table 6-4.	Repair/replace defective components
	5. No TX injection	Check that RF level at jct. R100/R101 per schematic.	Check U251, L291-292, C290-291.
	6. No 5T source	Verify Q312 gate is 0 V dc in TX Verify Q312 drain is 5 V dc in TX.	Check/replace Q313. Check for shorts, check/replace Q312.
	7. TX gain stage failure	Check RF levels at Q100 and U110 per schematic.	Troubleshoot Q100/U110 and associated circuitry.
	8. Antenna switch failure	Verify dc voltage at jct. R122/L120 is approx 1.5 V.	Check/replace D120-121, L120-121, R120-122, etc.

Table 6-3. Troubleshooting Table for Transmitter (Continued)

Symptom	Possible Causes	Procedure	Corrective Action
Low Power	1. Low TX injection	Check that RF level at jct. R100/ R101 per schematic.	Check U251, L291-292, C290-291.
	2. Low gain in TX stage	Verify dc voltage at Q100-E is ~1.3 V (VHF) or ~0.5 V (UHF). Verify that RF level at U110-1 is approx. 1 V (VHF) or 1.6 V (UHF).	Verify 5T voltage is correct. Troubleshoot Q100 circuitry. Troubleshoot Q100 circuitry. Check/replace Q100.
	3. Incorrect control voltage	Verify that the dc voltage at PWR_SET (R162) is approx 1.8 V dc (at 1 watt) to 2.6 V dc (at 4-5 watts). Verify that the dc voltage at U110-2 is approx 2-3 V dc (at 1 watt) to 3-4 V dc (at 4-5 watts). (See schematic.)	Check programming. Troubleshoot controller circuitry. Check/ replace U451. Troubleshoot U150, Q150 and associated circuitry.
	4. Antenna switch defect	Verify dc voltage at jct. R122/L120 (VHF) or R121/L120 (UHF) is approx 1.7 V. *Note: Do not attempt to measure RF or DC voltages at the diodes. Damage to test equipment may occur.*	Check/replace D120-121, L120-121, R120-122, etc.
	5. Harmonic filter defect	Visually inspect components C130-137, L130-132. Check dc continuity of L130-132 *in RX mode only*.	Repair/replace if necessary.
Poor TX range, conducted power OK	1. RF test jack defective	Verify continuity of J140 pins 3 and 4 *in RX mode only*.	Replace J140.
	2. Antenna matching network fault	Visually inspect components C140-141, L140 or L141. Check dc continuity of L140 or L141*in RX mode only*.	Repair/replace if necessary.
	3. Defective or wrong antenna	Verify correct antenna is installed. Try another antenna.	Replace antenna.
No internal mic audio (EXT MIC audio OK)	1. Mic bias fault	Verify U451-35 is low when side PTT is pressed. Verify Q470-6 is high when side PTT button is pressed.	Check/replace U451. Check/replace R474, R476, and Q470.
	2. Defective mic	Verify approx 1.8 V dc across cartridge when side PTT button is pressed. Verify audio present (~10 mV rms) when speaking into mic.	Check mic connector and R478. Replace mic cartridge.
	3. Defective mic jack	Verify continuity between J471 pins 4 and 5.	Replace J471.

Table 6-3. Troubleshooting Table for Transmitter (Continued)

Symptom	Possible Causes	Procedure	Corrective Action
No EXT MIC audio	1. Mic bias fault	Verify approx 1.8 V dc across EXT MIC cartridge in TX mode. Verify audio present (~10 mV rms) when speaking into mic.	Check Q470. R475, R477, L471. Check VR473, VR475, D470 for shorts.
	2. Audio path fault	Verify mic audio present (~10 mV rms) at U451-46. Verify amplified mic audio present (~200 mV rms) at U451-40.	Check L471, C470. Check/replace U451.
	3. Defective audio accessory	Try another accessory.	Replace defective accessory.

6.4 Troubleshooting Table for Board and IC Signals

Table 6-4. Troubleshooting Table for Board and IC Signals

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U51 IFIC	1	RF input 44.85 MHz	1.20	
	2	RF input decoupling	1.20	
	3	2nd LO osc output	4.02	
	4	2nd LO osc input	4.60	
	5	RSSI output	0.74	(no received signal)
	6	Vcc	4.70	
	7	Audio feedback	0.89	
	8	Audio output	1.44	DEMOD to stage U510
	9	RSSI feedback	0.74	(no received signal)
	10	Quad detector input	2.22	
	11	Limiter output	1.25	
	12	Limiter decoupling 2	1.30	
	13	Limiter decoupling 1	1.30	
	14	Limiter input	1.28	
	15	Ground	GND	
	16	IF amp output	1.22	
	17	IF amp decoupling 2	1.26	
	18	IF amp input	1.26	
	19	IF amp decoupling 1	1.26	
	20	2nd mixer output	3.09	
U52 BW Select Switch	1	Inverter 1 input	0	(25 kHz mode)
	2	Inverter 2 output	0	(25 kHz mode)
	3	Inverter 3 input (NU)	GND	
	4	Ground	GND	
	5	Inverter 3 output (NU)	4.96	
	6	Inverter 2 input	3.00	(25 kHz mode)
	7	Inverter 1 output	4.95	(25 kHz mode)
	8	Vcc	4.96	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U110 RF Power Amp	1	RF input	0	(TX mode)
	2	Vgg (gate bias)	2.65 (typ)	(TX mode) (4.25 V typ at VHF)
	3	Vdd	6.59	(TX mode)
	4	RF output	--	Do not measure
	5	Ground	GND	
U150 Dual Opamp	1	Unit 1 output	4.20 (typ)	(TX mode) (5.8 V typ at VHF)
	2	Unit 1 (-) input	2.39 (typ)	(TX mode)
	3	Unit 1 (+) input	2.39 (typ)	(TX mode)
	4	Ground	GND	
	5	Unit 2 (+) input	3.30 (typ)	(TX mode)
	6	Unit 2 (-) input	3.35 (typ)	(TX mode)
	7	Unit 2 output	2.23 (typ)	(TX mode)
	8	Vcc	6.79	(TX mode)
U201 Freq Synthesizer	1	AUX2 output (NU)	0	
	2	AUX3 output (TRB)	0.03	To U251-19 (RX mode)
	3	AUX4 output (NU)	0	
	4	Lock detect output	2.98	To U401-56
	5	PD Vdd	2.98	
	6	Digital ground	GND	
	7	Serial data input	3.23	
	8	Serial clock input	0	
	9	Synth chip select	3.23	From U401-47
	10	Modulation input	1.50	From U451-40
	11	VMULT4 (NU)	2.98	
	12	VMULT3 (NU)	0	
	13	VRO	4.96	
	14	VMULT2	1.49	
	15	VMULT1	1.49	
	16	INDMULT (NU)	0	
	17	NC1	0	
	18	Ref select (NU)	0	
	19	Buffered 16.8 MHz out	1.54	
	20	Analog Vdd	3.00	
	21	V bypass (NU)	1.55	
	22	Analog ground	GND	
	23	Ref osc XTAL1	2.07	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U201 Freq Synthesizer	24	Ref osc XTAL2	0	
	25	Ref osc warp output	3.00	
	26	Superfilter cap	4.48	
	27	Superfilter base (NU)	3.76	
	28	Superfilter output	4.52	
	29	NC2	0	
	30	Superfilter input	4.96	
	31	NC3	0	
	32	Prescaler input	1.97	
	33	Prescaler ground	GND	
	34	Prescaler Vdd	2.99	
	35	Prescaler Vref (NU)	1.97	
	36	Digital Vdd	2.99	
	37	TEST1 (NU)	0.01	
	38	TEST2 (NU)	0	
	39	Bias 2	3.38 (typ)	(1.34 V in TX mode)
	40	Bias 1	1.50 (typ)	(3.20 V in TX mode)
	41	Modulation output	3.42 (typ)	(1.62 V typ in TX mode)
	42	CCOMP (NU)	0.05	
	43	Steering line IOUT	9.62 (typ)	Depends on frequency
	44	PD ground	GND	
	45	Steering line IADAPT	9.62 (typ)	Depends on frequency
	46	Adapt switch (NU)	0	
	47	Voltage from charge pump	12.8	
	48	AUX1 output (NU)	2.98	
U251 VCO / Buffer	1	TX VCO current adjust	4.50	
	2	RX VCO current adjust	4.35	
	3	Superfiltered input	4.51	
	4	Collector RF in amp	4.35	
	5	RX VCO base	1.27	
	6	RX VCO emitter	0.48	
	7	RX switch output (NU)	0	
	8	RX buffered VCO output	3.36	
	9	GND_FLAG	GND	
	10	TX buffered VCO output	3.36	
	11	GND_BUFFERS	GND	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U251 VCO / Buffer	12	Prescaler output	2.26	
	13	TX switch output (NU)	0.06	
	14	Vcc_BUFFERS	3.00	
	15	TX VCO emitter	0	(RX mode)
	16	TX VCO base	0	(RX mode)
	17	GND_LOGIC	GND	
	18	Vcc_LOGIC	3.00	
	19	TRB input	0.03	From U201-2 (RX mode)
	20	FLIP input	GND	
U310 5 V Regulator	1	Vin	7.48	
	2	Ground	GND	
	3	Control input	7.48	
	4	Bypass capacitor	1.26	
	5	Vout	4.96	
U320 3.3 V Regulator	1	Ground	GND	
	2	Feedback	1.23	
	3	Tap (NU)	0	
	4	Vin	7.48	
	5	Vout	3.23	
	6	Sense (NU)	0	
	7	Error (reset output)	3.20	
	8	Shutdown input	7.48	
U330 3 V Regulator	1	Vin	7.48	
	2	Ground	GND	
	3	Control input	7.48	
	4	Bypass capacitor	1.26	
	5	Vout	3.00	
U401 Microprocessor	1	PD4_SCK serial clock input	0	
	2	PD5_SS	3.23	ASFIC chip select
	3	PD6_VLIN	3.23	EEPROM chip select
	4	PG7_R_W	3.21	
	5	PG6_AS	3.23	
	6	PG0_XA13	3.23	
	7	PB7_ADDR15	0.026	
	8	PB6_ADDR14	0.028	
	9	PB3_ADDR11	3.06	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	10	PB1_ADDR9	3.05	
	11	PB2_ADDR10	0.16	
	12	VDD	3.23	
	13	VSS	GND	
	14	PBO_ADDR8	3.05	
	15	PB5_ADDR13	0.13	
	16	PG1_XA14	0.20	
	17	PG4_XA17	3.17	
	18	PG5_XA18	0	
	19	PG3_XA16	3.21	
	20	PG2_XA15	0.30	
	21	PB4_ADDR12	0.22	
	22	PF7_ADDR7	3.03	
	23	PF6_ADDR6	3.08	
	24	PF5_ADDR5	3.06	
	25	PF4_ADDR4	0.16	
	26	PF3_ADDR3	0.26	
	27	PF2_ADDR2	3.06	
	28	PF1_ADDR1	3.06	
	29	PFO_ADDR0	3.05	
	30	PC0_DATA0	0.69	
	31	PC1_DATA1	0.96	
	32	PC2_DATA2	1.10	
	33	PC3_DATA3	0.81	
	34	PC4_DATA4	0.62	
	35	PC5_DATA5	0.68	
	36	PC6_DATA6	0.67	
	37	PC7_DATA7	0.73	
	38	PH7_CSPROG	3.05	
	39	VDDL	3.23	
	40	VSSL	GND	
	41	PH6_CSGP2	3.23	
	42	PH5_CSGP1	3.23	
	43	PH4_CSIO	0	
	44	PH3_PW4	3.21	On/off control output
	45	PH2_PW3	0	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	46	PH1_PW2	3.00	
	47	PH0_PW1	3.23	Synth chip select
	48	XIRQ	3.00	
	49	PI7	1.48	RX enable
	50	PI6	0.01	TX enable
	51	PI5	3.23	
	52	PI4	0	Green LED enable
	53	PI3	0	Red LED enable
	54	PI2	0	
	55	PI1	0	
	56	PI0	2.98	Lock detect from U201-4
	57	MODB_VSTBY	3.22	Boot mode enable
	58	MODA_LIR	3.12	
	59	AVDD	3.23	
	60	PE7_AN7	3.20	
	61	PE6_AN6	3.20	
	62	PE5_AN5	2.91	VOX threshold detect
	63	PE4_AN4	0.73	RSSI input
	64	PE3_AN3	0.14	
	65	PE2_AN2	1.62	
	66	PE1_AN1	0 - 3.3 V	Volume control wiper
	67	PE0_AN0	2.48	33% of battery voltage
	68	VRL	0	
	69	VRH	3.20	
	70	AVSS	GND	
	71	PJ0_CSGP3	3.23	Side PTT button
	72	PJ1_CSGP4	0	External MIC PTT
	73	PJ2	3.23	
	74	PJ3	3.23	
	75	PJ4	3.23	
	76	PJ5	0	
	77	PJ6	3.23	Bottom option button
	78	PJ7	3.23	Top option button
	79	PA0_IC3	0	
	80	PA1_IC2	1.57	
	81	PA2_IC1	3.00	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	82	PA3_IC4_OC5_OC1	3.00	
	83	PA4_OC4_OC1	0	Squelch detect input
	84	PA5_OC3_OC1	0	Channel activity input
	85	PA6_OC2_OC1	0	
	86	PA7_PA1_OC1	0	
	87	VSSR	GND	
	88	VDDR	3.23	
	89	ECLK (NU)	1.60	
	90	EXTAL	1.70	Clock from U451-28
	91	XTAL	1.40	Not used
	92	VDDSYN	0	
	93	XFC (NU)	0	
	94	RESET	3.20	From U320
	95	LVOUT	0	
	96	IRQ	3.20	
	97	PD0_RXD	3.23	
	98	PD1_TXD	1.9	
	99	PD2_MISO	0	
	100	PD3_MOSI	3.23	
U402 EEPROM	1	Chip select	3.23	From U401-3
	2	Serial data out	0	
	3	Write protect	3.23	
	4	Vss	GND	
	5	Serial data in	3.23	
	6	Serial clock	0	
	7	Hold	3.23	
	8	Vcc	3.23	
U404 Flash ROM	1	A11	3.06	
	2	A9	3.08	
	3	A8	3.05	
	4	A13	0.13	
	5	A14	0.31	
	6	NC	3.17	
	7	EN_WE	3.21	From U401-4
	8	Vcc	3.23	
	9	RESET	3.20	

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U404 Flash ROM	10	A16	3.17	
	11	A15	0.30	
	12	A12	0.22	
	13	A7	3.03	
	14	A6	3.08	
	15	A5	3.06	
	16	A4	0	
	17	A3	0.24	
	18	A2	3.08	
	19	A1	3.05	
	20	A0	3.05	
	21	D0	0.69	
	22	D1	0.94	
	23	D2	1.08	
	24	GND	GND	
	25	D3	0.78	
	26	D4	0.59	
	27	D5	0.66	
	28	D6	0.67	
	29	D7	0.75	
	30	EN_CE	3.01	From U401-38
	31	A10	0.16	
	32	EN_OE	0	From U401-86
U451 ASFIC_CMP	1	VDD for analog circuits	3.00	
	2	DISC audio input	1.34	From U510
	3	Ground for analog circuits	GND	
	4	DACU output	0	
	5	DACR output	0	
	6	DACG output	2.38 (typ)	Power set (TX mode)
	7	VOX peak detector output	2.91	
	8	PLCAP for DC integrator	0.40	
	9	SQIN	0.01	
	10	Universal audio input/output	0	
	11	VDD for DACs	4.95	
	12	SQCAP	0	
	13	GCB2 general purpose output	0	Audio PA_EN (unsquelched)

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U451 ASFIC_CMP	14	GCB1 general purpose output	0	
	15	GCB0 general purpose output	3.00	BW select (25 kHz mode)
	16	Squelch channel activity output	0	To U401-84
	17	Squelch detect digital output	0	To U401-83
	18	PL/low speed data I/O	1.50	
	19	High speed data I/O	3.00	
	20	Chip select	3.23	From U401-2
	21	Serial clock input	0	
	22	Serial data input	3.23	
	23	Ground for clock synthesizer	GND	
	24	Loop filter cap for clock syn	0.74	
	25	PLCAP2 for LS integrator	1.17	
	26	Not used	0	
	27	Vdd for clock synthesizer	3.00	
	28	Clock synthesizer output	1.70	
	29	1200 Hz ref for MDC decode	3.00	
	30	GNDDO	GND	
	31	Ground for digital circuits	GND	
	32	Vdd for analog switches	4.96	
	33	Vdd for digital circuits	3.00	
	34	16.8 MHz master clock input	1.54	
	35	GCB3 general purpose output	3.00	Internal MIC enable
	36	TX audio return from option	0	
	37	GCB4 general purpose output	0	
	38	GCB5 general purpose output	0	
	39	RX audio send to option	1.48	
	40	Modulation output	1.50	To U201-10
	41	RX audio out to power amp	1.51	
	42	Flat TX audio return from option	0.20	
	43	RX audio return to option	1.50	
	44	Flat TX audio send to option	1.50	
	45	Vdd for audio path I/O filters	3.00	
	46	Mic audio input	1.50	
	47	Ground for audio path I/O filters	GND	
	48	Ext mic audio input (not used)	0	

Notes:

Table 6-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U480 Dual Opamp	1	Unit 1 output	2.48	
	2	Unit 1 (-) input	2.48	
	3	Unit 1 (+) input	2.46	
	4	Ground	GND	
	5	Unit 2 (+) input	0.28	
	6	Unit 2 (-) input	0.29	
	7	Unit 2 output	0	
	8	Vcc	4.96	
U490 Audio Power Amp	1	Enable/shutdown	0.12	(Unsquelched)
	2	Bias reference	3.26	(Unsquelched)
	3	(+) input	3.26	(Unsquelched)
	4	(-) input	3.27	(Unsquelched)
	5	(-) output	3.25	(Unsquelched)
	6	Vcc	7.48	(Unsquelched)
	7	Ground	GND	
	8	(+) output	3.29	(Unsquelched)
U510 Dual Opamp	1	Unit 1 output	1.75	
	2	Unit 1 (-) input	1.56	
	3	Unit 1 (+) input	1.55	
	4	Ground	GND	
	5	Unit 2 (+) input	1.55	
	6	Unit 2 (-) input	1.56	
	7	Unit 2 output	1.38	
	8	Vcc	4.96	

1. All voltages are measured with a high-impedance digital voltmeter and expressed in volts DC relative to ground (0 V).
2. Voltages are measured with a DC input voltage of 7.50 + .02 volts DC applied to the battery connector (J301).
3. All voltages are measured in the squelched receive mode, unless otherwise indicated.
4. Voltages are identical for VHF and UHF models unless otherwise indicated.

Chapter 7 VHF Schematic Diagrams, Overlays, and Parts Lists

7.1 Introduction

This section provides schematic diagrams, overlays, and parts lists for the radio circuit boards and interface connections.

7.1.1 Notes For All Schematics and Circuit Boards

* Component is frequency sensitive. Refer to the Electrical Parts List for value and usage.

1. Unless otherwise stated, resistance values are in ohms (K = 1000), capacitance values are in picofarads (pF) or microfarads (µF), and inductance values are in nanohenries (nH) or microhenries (µH).
2. DC voltages are measured from point indicated to chassis ground using a Motorola DC multimeter or equivalent. If the board has been removed from the chassis, the transmitter module mounting screws may be used for ground connection. (*Note: The antenna nut bracket is not connected to ground.*) Operating mode dependent voltages are followed by (RX) for receive mode, (TX) for transmit mode, (UNSQ) for unsquelched mode, etc.
3. RF voltages on VHF models are measured with a Fluke model 85 RF probe. The indicated voltages expressed in mV (RF) are DC level readings which correspond approximately 1:1 to the RF voltage level in mV rms. RF voltages in the Receiver Front End and Receiver Back End circuits are measured with an on-channel 100 mV (-7 dBm) RF signal applied to the antenna jack J140.
4. RF voltages on UHF models are measured both with a high-impedance RF voltmeter having a bandwidth in excess of 500 MHz (levels are expressed in dBm) and with a Fluke model 85 RF probe [levels are expressed in mV (RF)]. These indicated voltages are DC level readings which correspond approximately 1:1 to the RF voltage level in mV rms, and are only approximate for UHF frequency measurements. RF voltages in the Receiver Front End and Receiver Back End circuits are measured with an on-channel 100 mV (-7 dBm) RF signal applied to the antenna jack J140.
5. Audio voltages are measured with a high-impedance AC rms voltmeter. The indicated voltages are expressed in mV rms. Receive mode voltages are followed by (RX) and are measured with an on-channel signal with 1 kHz modulation at 60% deviation (3 kHz for 25 kHz channels, or 1.5 kHz for 12.5 kHz channels). Transmit mode voltages are followed by (TX) and are measured with a 1 kHz, 10 mV rms signal present at the external microphone input (accessory connector J471 pin 4 hot and pin 7 ground).
6. Reference Designators are assigned in the following manner:

Ref. No. Series	Circuit Block
1-99	RF Front End
100-149	Transmitter RF Stages
150-200	Transmitter Power Control
201-250	Frequency Synthesizer
251-300	VCO

Ref. No. Series	Circuit Block
301-400	DC Regulation
401-450	Microprocessor
451-550	Audio

7. Circuit Block Interconnection Legend:

Name	Description
USWB+	Unswitched Battery Voltage (always on)
5V	5 volts (regulated)
5R	5 volts in RX mode only
5T	5 volts in TX mode only
RESET	Low-line reset signal from U320 to uP
D3_3V	Digital 3.3 volts (regulated)
3V	Analog 3 volts (regulated)
TX_ENA	Transmit enable signal from uP to transmitter
PWR_SET	DC voltage from ASFIC to TX power control
DEMOD	RX audio from backend to ASFIC
BW_SEL	Backend filter BW select from ASFIC
RSSI	RX signal strength indication from IFIC to uP
IF_IN/OUT	44.85 MHz from 1st mixer to high IF filter
RF_IN/OUT	RX signal from antenna switch to front end
MOD OUT/IN	TX modulation from ASFIC to synthesizer
16_8_MHZ	Ref osc signal from synthesizer to ASFIC
SYNTH_CS	Synthesizer chip select from uP
SPI_CLK	Serial clock from uP
SPI_DATA_OUT	Serial data from uP
LOCK	Lock detect indication from synth to uP
PRESC	VCO freq feedback from VCOBIC to synth
V_STEER	Steering line voltage from synth to VCO's
V_SF	Super-filtered 4.5 volts from synth to VCOBIC
VCO_MOD	TX modulation from ASFIC to synthesizer
TRB	TX/RX control from synth to VCOBIC
RX_INJ	Buffered RX VCO output to RX 1st mixer
TX_INJ	TX VCO output to transmitter input

7.1.2 Six Layer Circuit Board

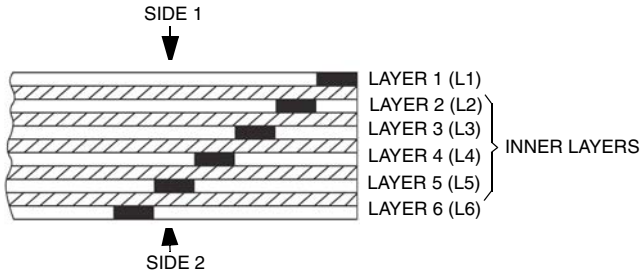

Figure 7-1. Six-Layer Circuit Board: Copper Steps in Layer Sequence

7.2 Speaker and Microphone Schematic

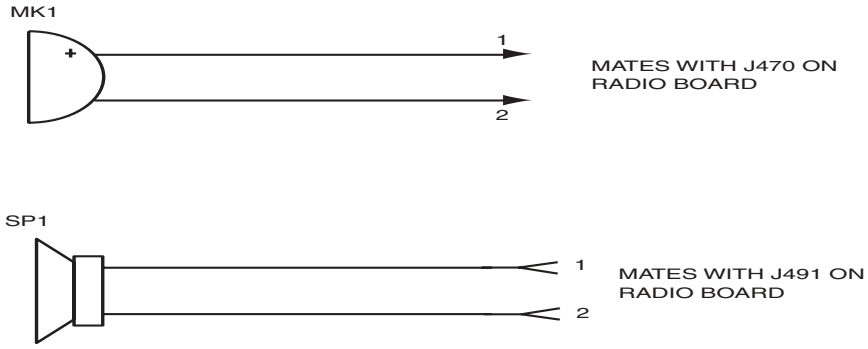

Figure 7-2. Speaker and Microphone Schematic

7.2.1 Speaker and Microphone Parts List

Reference Designator	Motorola Part No.	Description
MK1	5085880L01	Microphone, electret
SP1	5085738Z08	Speaker assembly with connector

Notes:

Chapter 8 403-440 MHz UHF Theory Of Operation

8.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Chapter 13 of this manual.

8.2 UHF Receiver

The UHF receiver covers the range of 403-440 MHz and provides switchable IF bandwidth for use with 20/25/30 kHz or 12.5 kHz channel spacing systems. The receiver is divided into two major blocks, as shown in Figure 8-1.

- Front End
- Back End

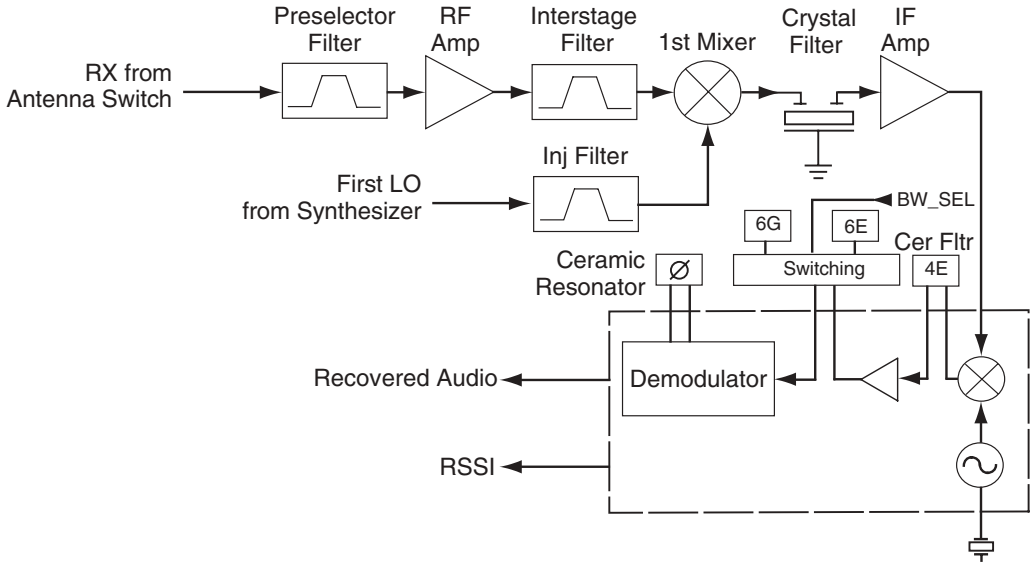

Figure 8-1. UHF Receiver Block Diagram

8.2.1 Receiver Front End

Incoming RF signals from the antenna are first routed through the harmonic filter and antenna switch, part of the transmitter circuitry, before being applied to the receiver front end. The receiver front end consists of a preselector filter, RF amplifier, an interstage filter, and a double-balanced first mixer.

The preselector filter is a fixed-tuned 3-pole Butterworth design using discrete elements (L1-L3, C1-C10, C12 and C523) in a shunt-resonator configuration. It has a 3 dB bandwidth of 68 MHz centered at 421 MHz, an insertion loss of 2.2 dB and image attenuation of 38 dB at 350 MHz. Diode CR1 protects the RF amplifier by limiting excessive RF levels. The filter bandwidth is considerably wider than the receive band, to achieve low insertion loss in a compact size. C523 provides a transmission-zero to improve image attenuation.

The output of the filter is matched to the base of RF amplifier Q21, which provides 18 dB of gain and a noise figure of 4 dB. A BFS505 device is used for high gain, low noise figure and reduced operating current. Operating voltage is obtained from the 5R source, which is turned off during transmit to reduce dissipation in Q21. Current mirror Q22 maintains the operating current of Q21 constant at 8 mA regardless of device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the interstage filter, a fixed-tuned 4-pole Butterworth shunt-coupled resonator design having a 3 dB bandwidth of 68 MHz centered at 462 MHz, and insertion loss of 3.5 dB. This filter yields an image rejection of 58 dB at 350 MHz, assisted by a transmission-zero at 300 MHz implemented by C524 for the reasons mentioned above.

The output of the interstage filter is connected to the passive double-balanced mixer consisting of components T41, T42, and CR41. This mixer has a conversion loss of 7.2 dB. Low-side injection from the frequency synthesizer is filtered by L40-L41 and C41-C45 to remove second harmonic energy that may degrade half-IF spurious rejection performance. The injection filter has a 3 dB bandwidth of 100 MHz centered at 376.15 MHz, and an insertion loss of 2.7 dB. The second-harmonic rejection is typically 45 dB or greater. The filtered injection signal is applied to T42 at a level of +6 dBm.

The mixer output is applied to a diplexer network (L51-L52, C51, R51) which matches the 44.85 MHz IF signal to crystal filter FL51, and terminates the mixer into 50Ω at all other frequencies.

8.2.2 Receiver Back End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL51, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of ±6.7 kHz, a maximum 20 dB bandwidth of + 12.5 kHz, and a maximum insertion loss of 3.5 dB. The output is matched to IF amplifier stage Q51 by L53 and C93. Q51 provides 16 dB of gain and a noise figure of 1.8 dB. The dc operating current is 1 mA. The output of Q51 is applied to the input of the receiver IFIC U51. Diode CR51 limits the maximum RF level applied to the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency, 44.395 MHz, is determined by Y51. The second mixer converts the 44.85 MHz high IF frequency to 455 kHz.

Additional IF selectivity is provided by two ceramic filters, FL52 (between the second mixer and IF amp) and FL53 or FL54 (between the IF amp and the limiter input). The wider filter FL53 is used for 20/25 kHz channel spacing, and the narrower filter FL54 is used for 12.5 kHz channels. When the BW_SEL line is high, the two upper diodes in packages D51 and D52 are forward biased, selecting FL53 for 20/25 kHz channels. When the BW_SEL line is low, the two lower diodes in packages D51 and D52 are forward biased, selecting FL54 for 12.5 kHz channels.

The ceramic filters have the following specifications:

	FL52	**FL53**	**FL54**
Number of Elements:	4	6	6
Insertion Loss:	4 dB	4 dB	4 dB
6 dB Bandwidth:	15 kHz	15 kHz	9 kHz
50 dB Bandwidth:	30 kHz	30 kHz	22 kHz
Stopband Rejection:	27 dB	47 dB	47 dB

Ceramic resonator Y70 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q70 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering the distortion of the recovered audio signal. The recovered audio level at the DEMOD output is 120 mV rms (25 kHz channel, 3 kHz deviation) or 60 mV rms (12.5 kHz channel, 1.5 kHz deviation). An additional RSSI output provides a DC voltage level that is proportional to RF signal level. This voltage is measured by an A/D converter contained in the microprocessor (PE4_AN4, U401 pin 63).

8.3 UHF Transmitter

The UHF transmitter covers the range of 403-440 MHz. Depending on model, the output power of the transmitter is either switchable on a per-channel basis between high power (4 watts) and low power (1 watt), or is factory preset to 2 watts. The transmitter is divided into four major blocks as shown in Figure 8-2.

- Power Amplifier
- Harmonic Filter
- Antenna Matching Network
- Power Control.

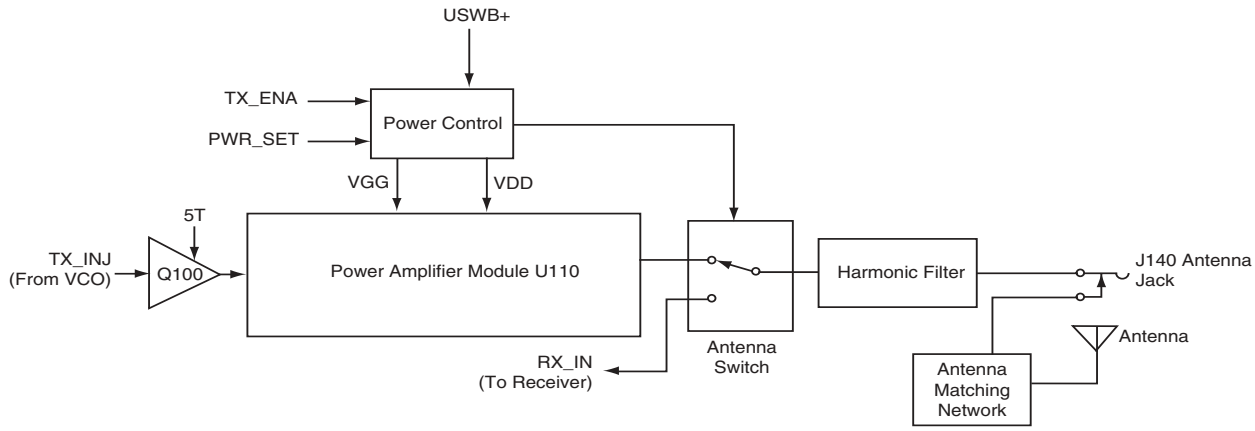

Figure 8-2. UHF Transmitter Block Diagram

8.3.1 Transmitter Power Amplifier

The transmitter power amplifier has three stages of amplification. The first stage, Q100, operates in Class A from the 5T source. It provides 17 dB of gain and an output of 50 mW. The current drain is typically 35mA. Components C105, C107 and L103 match the output of Q100 to the 50Ω input of the module U110.

U110 is a two stage Silicon MOS FET power amplifier module. Drain voltage is obtained from UNSW B+ after being routed through current-sense resistor R150 in the power control circuit. The output power of the module is controlled by varying the DC gate bias on U110 pin 2 (VGG).

8.3.2 Antenna Switch

The antenna switch consists of two pin diodes, D120 and D121. In the receive mode, both diodes are off. Signals applied at the antenna or at jack J140 are routed, via the harmonic filter, through network C122-C124 and L121, to the receiver input. In the transmit mode, Q170 is on and TXB+ is present, forward-biasing both diodes into conduction. The diode current is 20 mA, set by R120-R121. The transmitter RF from U110 is routed through D120, and via the harmonic filter to the antenna jack. D121 conducts, shunting RF power and preventing it from reaching the receiver. L121 is selected to appear as a 1/4 wave at UHF, so that the low impedance of D121 appears as a high impedance at the junction of D120 and the harmonic filter input. This provides a high series impedance and low shunt impedance divider between the power amplifier output and receiver input.

8.3.3 Harmonic Filter

The harmonic filter consists of components C122 (Range 1 UHF) C136 and L130-L132. The harmonic filter is a seven-pole Chebychev low-pass configuration, optimized for low insertion loss, with a 3 dB frequency of approximately 600 MHz and typically less than 0.8 dB insertion loss in the passband.

8.3.4 Antenna Matching Network

The harmonic filter presents a 50Ω impedance to antenna jack J140. A matching network, made up of C140-C141 and L140, is used to match the antenna impedance to the harmonic filter. This optimizes the performance of the transmitter and receiver into the impedance presented by the antenna, significantly improving the antenna's efficiency.

8.3.5 Power Control

The power control circuit is a dc-coupled amplifier whose output is the dc gate bias voltage (VGG) applied to the two stages of the RF power amplifier U110.

The output power of the transmitter is adjusted by varying the setting of the power-set DAC contained in the ASFICcmp IC (DACG, U451 pin 6). This PWR_SET voltage is applied to U150 pin 3.

Stage U150-2 compares the voltage drop across current sense resistor R150 to the voltage drop across resistor R151 caused by current flow through Q150, and adjusts its output (pin 7) to maintain equal voltages at pins 5 and 6. Thus the current flow through Q150, and hence its emitter voltage, is proportional to the current drawn by stage U110, which is in turn proportional to the transmitter output power. The emitter voltage of Q150 is applied to U150 pin 2, where it is compared to the power set voltage PWR_SET at pin 3.

The output of U150 pin 1 is divided by R110 and R111 and applied as a gate voltage to the power amplifier U110. By varying this gate voltage as needed to keep the voltages at U150 pins 2 and 3 equal, power is maintained at the desired setting. Excessive final current, for example due to antenna mismatch, causes a lowering of the voltage at U150 pin 6, an increased voltage at pin 2, and a lowering of the voltage at pin 1 and of the gate voltage VGG. This prevents damage to the final stage due to excessive current.

8.4 UHF Frequency Generation Circuitry

The frequency generation system, shown in Figure 8-3, is composed of two circuit blocks, the Fractional-N synthesizer IC U201, the VCO/Buffer IC U251, and associated circuitry. Figure 8-4 shows the peripheral interconnect and support circuitry used in the synthesizer block, and Figure 8-5 details the internal circuitry of the VCOBIC and its interconnections to the surrounding components. Refer to the schematic to identify reference designators.

The Fractional-N synthesizer is powered by regulated 5 V and 3 V provided by U310 and U330 respectively. 5 V is applied to U201 pins 13 and 30, and 3 V is applied to pins 5, 20, 34 and 36. The synthesizer in turn generates a super-filtered 4.5 V supply (VSF, from pin 28) to power U251. In addition to the VCO, the synthesizer also interfaces with the logic and ASFICcmp circuits. Programming for the synthesizer is accomplished through the microprocessor SPI_DATA_OUT,

SPI_CLK, and SYNTH_CS (chip select) lines (U409 pins 100, 1 and 47 respectively). A logic high (3 V) from U201 pin 4 indicates to the microprocessor that the synthesizer is locked.

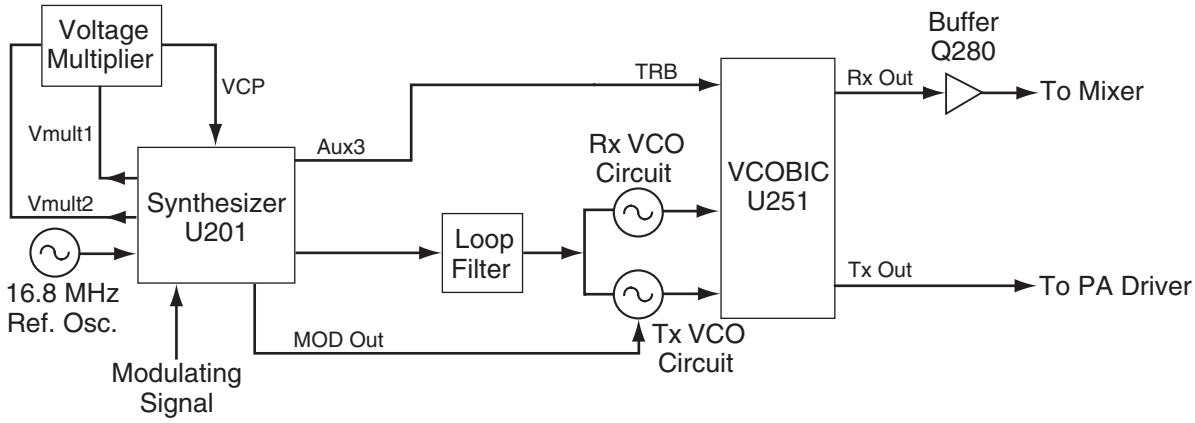

Figure 8-3. UHF Frequency Generation Unit Block Diagram

Transmit modulation from the ASFICcmp (U451 pin 40) is applied to U201 pin 10 (MOD_IN). An electronic attenuator in the ASFICcmp adjusts overall transmitter deviation by varying the audio level applied to the synthesizer IC. Internally the audio is digitized by the Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio is also routed through an internal attenuator for the purpose of balancing the low port and high port modulation and reducing the deviation by 6 dB for 12.5 kHz channels, and is available at U201 pin 41 (VCO_MOD). This audio signal is routed to the VCO's modulator.

8.4.1 Fractional-N Synthesizer

The Fractional-N synthesizer, shown in Figure 8-4, uses a 16.8 MHz crystal (Y201) to provide the reference frequency for the system. External components C201-C203, R202 and D201 are also part of the temperature-compensated oscillator circuit. The dc voltage applied to varactor D201 from U201 pin 25 is determined by a temperature-compensation algorithm within U201, and is specific to each crystal Y201, based on a unique code assigned to the crystal that identifies its temperature characteristics. Stability is better than 2.5 ppm over temperatures of -30 to 60°C. Software-programmable electronic frequency adjustment is achieved by an internal DAC which provides a frequency adjustment voltage from U201 pin 25 to varactor D201.

The synthesizer IC U201 further divides the 16.8 MHz signal to 2.1 MHz, 2.225 MHz, or 2.4 MHz for use as reference frequencies. It also provides a buffered 16.8 MHz signal at U201 pin 19 for use by the ASFICcmp.

To achieve fast locking of the synthesizer, an internal adapt charge pump provides higher current at U201 pin 45 to quickly force the synthesizer within lock range. The required frequency is then locked by the normal mode charge pump at pin 43. A loop filter (C243-C245 and R243-R245) removes noise and spurs from the steering voltage applied to the VCO varactors, with additional filtering located in the VCO circuit.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C221-C224 and D220-D221. Two 3 V square waves from U201 pins 14-15 provide the drive signals for the voltage multiplier, which generates 12.1 V at U201 pin 47. This voltage is filtered by C225-C228.

One of the auxiliary outputs of the synthesizer IC (AUX3, U201 pin 2) provides the TRB signal which determines the operating mode of the VCO, either receive or transmit.

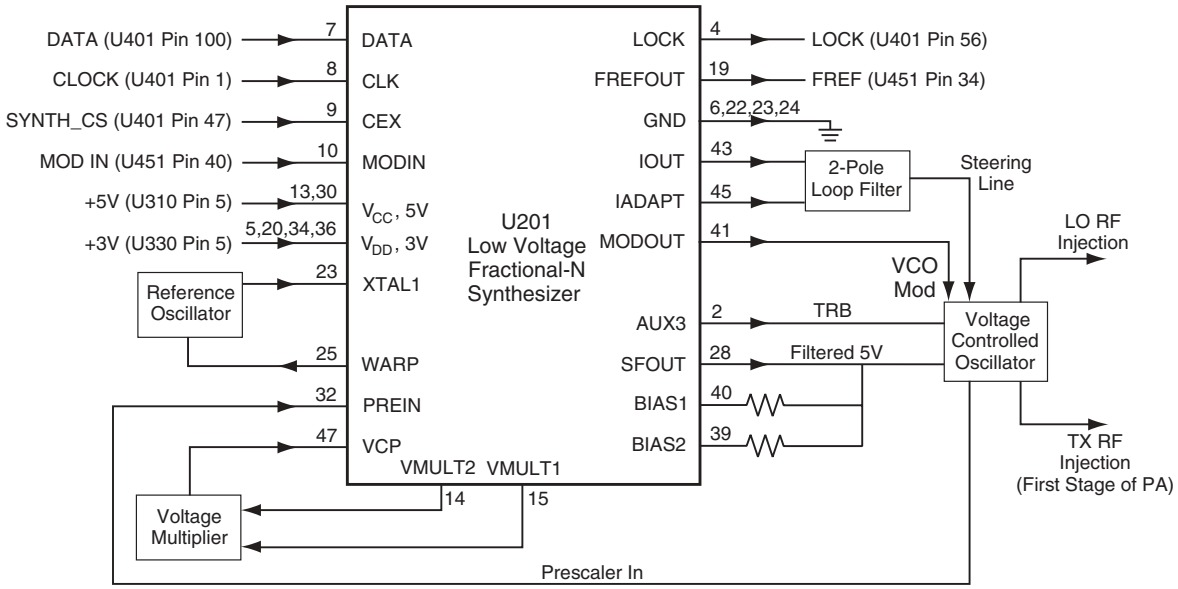

Figure 8-4. UHF Synthesizer Block Diagram

8.4.2 Voltage Controlled Oscillator (VCO)

The VCOBIC (U251), shown in Figure 8-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U251 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U251 pin 12 through a low pass filter, to the prescaler input of the synthesizer IC (U201 pin 32). After frequency comparison in the synthesizer, a resultant DC control voltage is used to steer the VCO frequency. When the PLL is locked on frequency, this voltage can vary between 3.5 V and 10 V. L251 and C252 further attenuate noise and spurs on the steering line voltage.

In the receive mode, the TRB line (U251 pin 19) is low. This activates the receive VCO and the receive buffer of U251, which operate within the range of 358.15 to 395.15 MHz. The VCO frequency is determined by tank inductor L254, C253-C257, and varactor D251. The buffered RF signal at U251 pin 8 is further amplified by Q280 and applied as RX_INJ to the low-pass injection filter in the receiver front end circuit.

In the transmit mode, U251-19 is driven high by U201 pin 2, enabling the transmit VCO and buffer. The 403-440 MHz RF signal from U251 pin 10 is applied as TX_INJ to the input of the transmitter circuit via matching network C290-C291 and L291. TX VCO frequency is determined by L264, C263-

C267, and varactor D261. High-port audio modulation from the synthesizer IC is applied as VCO_MOD to varactor D262 which modulates the transmit VCO.

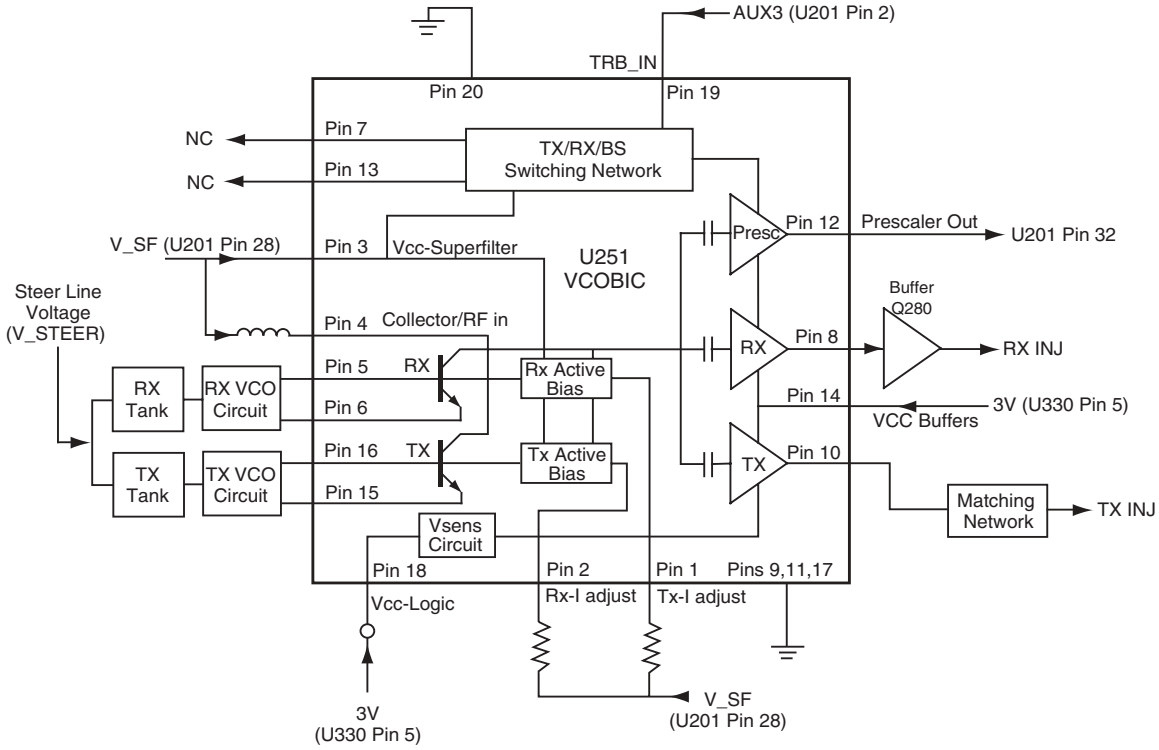

Figure 8-5. UHF VCO Block Diagram

8.5 Keypad

The keypad block diagram is shown in Figure 8-6. Pressing a key creates two distinct voltages KEYPAD_ROW and KEYPAD_COL. These voltages are sent directly to the radio's microprocessor on the main board. The microprocessor then interprets the voltage for KEYPAD_ROW and KEYPAD_COL for each key press.

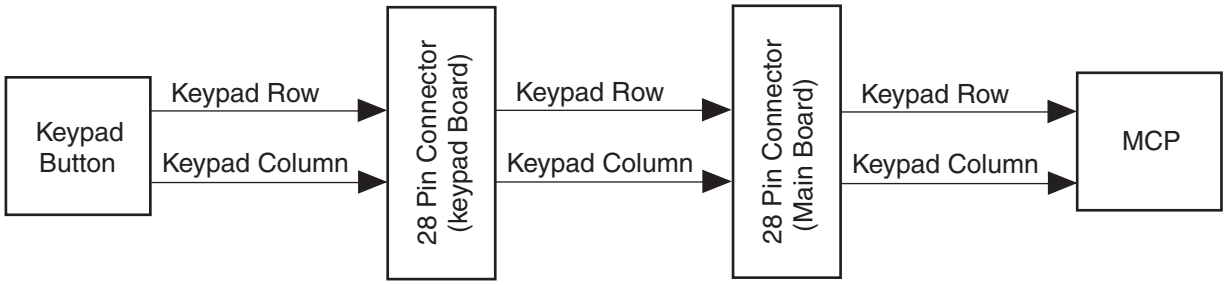

Figure 8-6. Keypad Block Diagram

Notes:

Chapter 9 438-470 MHz UHF Theory Of Operation

9.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Chapter 13 of this manual.

9.2 UHF Receiver

The UHF receiver covers the range of 438-470 MHz and provides switchable IF bandwidth for use with 20/25/30 kHz or 12.5 kHz channel spacing systems. The receiver is divided into two major blocks, as shown in Figure 9-1.

- Front End
- Back End

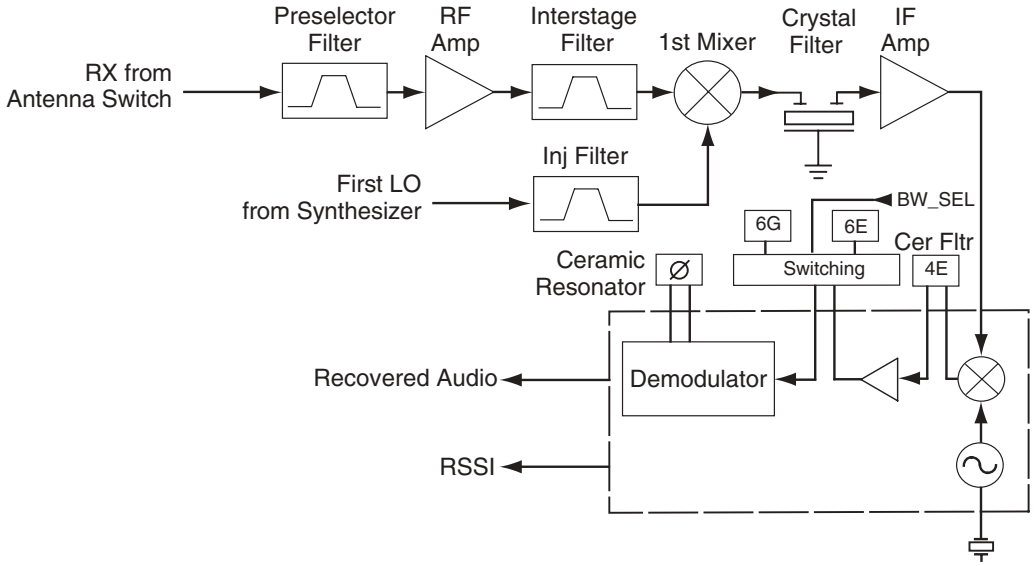

Figure 9-1. UHF Receiver Block Diagram

9.2.1 Receiver Front End

Incoming RF signals from the antenna are first routed through the harmonic filter and antenna switch, part of the transmitter circuitry, before being applied to the receiver front end. The receiver front end consists of a preselector filter, RF amplifier, an interstage filter, and a double-balanced first mixer.

The preselector filter is a fixed-tuned 3-pole Butterworth design using discrete elements (L1-L3, C1-C10, C12 and C523) in a shunt-resonator configuration. It has a 3 dB bandwidth of 68 MHz centered at 460 MHz, an insertion loss of 2 dB and image attenuation of 35 dB at 380 MHz. Diode CR1 protects the RF amplifier by limiting excessive RF levels. The filter bandwidth is considerably wider than the receive band, to achieve low insertion loss in a compact size. C523 provides a transmission-zero to improve image attenuation.

The output of the filter is matched to the base of RF amplifier Q21, which provides 18 dB of gain and a noise figure of 4 dB. A BFS505 device is used for high gain, low noise figure and reduced operating current. Operating voltage is obtained from the 5R source, which is turned off during transmit to reduce dissipation in Q21. Current mirror Q22 maintains the operating current of Q21 constant at 8 mA regardless of device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the interstage filter, a fixed-tuned 4-pole Butterworth shunt-coupled resonator design having a 3 dB bandwidth of 68 MHz centered at 462 MHz, and insertion loss of 3 dB. This filter yields an image rejection of 48 dB at 380 MHz, assisted by a transmission-zero at 300 MHz implemented by C524 for the reasons mentioned above.

The output of the interstage filter is connected to the passive double-balanced mixer consisting of components T41, T42, and CR41. This mixer has a conversion loss of 7.2 dB. Low-side injection from the frequency synthesizer is filtered by L40-L41 and C41-C45 to remove second harmonic energy that may degrade half-IF spurious rejection performance. The injection filter has a 3 dB bandwidth of 100 MHz centered at 408 MHz, and an insertion loss of 2 dB. The second-harmonic rejection is typically 40 dB or greater. The filtered injection signal is applied to T42 at a level of +6 dBm.

The mixer output is applied to a diplexer network (L51-L52, C51, R51) which matches the 44.85 MHz IF signal to crystal filter FL51, and terminates the mixer into 50Ω at all other frequencies.

9.2.2 Receiver Back End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL51, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of ±6.7 kHz, a maximum 20 dB bandwidth of + 12.5 kHz, and a maximum insertion loss of 3.5 dB. The output is matched to IF amplifier stage Q51 by L53 and C93. Q51 provides 16 dB of gain and a noise figure of 1.8 dB. The dc operating current is 1 mA. The output of Q51 is applied to the input of the receiver IFIC U51. Diode CR51 limits the maximum RF level applied to the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency, 44.395 MHz, is determined by Y51. The second mixer converts the 44.85 MHz high IF frequency to 455 kHz.

Additional IF selectivity is provided by two ceramic filters, FL52 (between the second mixer and IF amp) and FL53 or FL54 (between the IF amp and the limiter input). The wider filter FL53 is used for 20/25 kHz channel spacing, and the narrower filter FL54 is used for 12.5 kHz channels. When the BW_SEL line is high, the two upper diodes in packages D51 and D52 are forward biased, selecting FL53 for 20/25 kHz channels. When the BW_SEL line is low, the two lower diodes in packages D51 and D52 are forward biased, selecting FL54 for 12.5 kHz channels.

The ceramic filters have the following specifications:

	FL52	**FL53**	**FL54**
Number of Elements:	4	6	6
Insertion Loss:	4 dB	4 dB	4 dB
6 dB Bandwidth:	15 kHz	15 kHz	9 kHz
50 dB Bandwidth:	30 kHz	30 kHz	22 kHz
Stopband Rejection:	27 dB	47 dB	47 dB

Ceramic resonator Y70 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q70 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering the distortion of the recovered audio signal. The recovered audio level at the DEMOD output is 120 mV rms (25 kHz channel, 3 kHz deviation) or 60 mV rms (12.5 kHz channel, 1.5 kHz deviation). An additional RSSI output provides a DC voltage level that is proportional to RF signal level. This voltage is measured by an A/D converter contained in the microprocessor (PE4_AN4, U401 pin 63).

9.3 UHF Transmitter

The UHF transmitter covers the range of 438-470 MHz. Depending on model, the output power of the transmitter is either switchable on a per-channel basis between high power (4 watts) and low power (1 watt). The transmitter is divided into four major blocks as shown in Figure 9-2.

- Power Amplifier
- Harmonic Filter
- Antenna Matching Network
- Power Control.

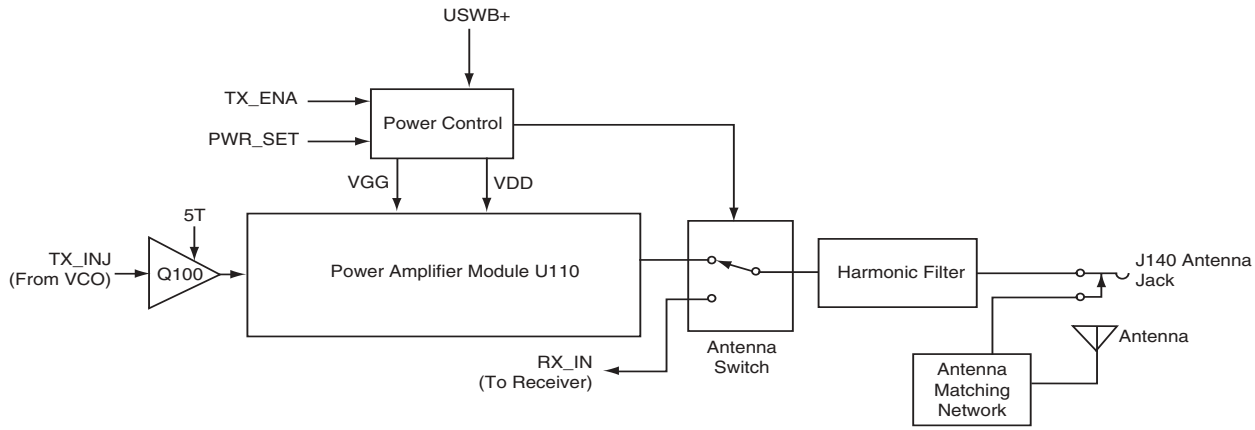

Figure 9-2. UHF Transmitter Block Diagram

9.3.1 Transmitter Power Amplifier

The transmitter power amplifier has three stages of amplification. The first stage, Q100, operates in Class A from the 5T source. It provides 17 dB of gain and an output of 50 mW. The current drain is typically 30mA. Components C105 and L103 match the output of Q100 to the 50Ω input of the module U110.

U110 is a two stage Silicon MOS FET power amplifier module. Drain voltage is obtained from UNSW B+ after being routed through current-sense resistor R150 in the power control circuit. The output power of the module is controlled by varying the DC gate bias on U110 pin 2 (VGG).

9.3.2 Antenna Switch

The antenna switch consists of two pin diodes, D120 and D121. In the receive mode, both diodes are off. Signals applied at the antenna or at jack J140 are routed, via the harmonic filter, through network C122-C124 and L121, to the receiver input. In the transmit mode, Q170 is on and TXB+ is present, forward-biasing both diodes into conduction. The diode current is 20 mA, set by R120-R121. The transmitter RF from U110 is routed through D120, and via the harmonic filter to the antenna jack. D121 conducts, shunting RF power and preventing it from reaching the receiver. L121 is selected to appear as a 1/4 wave at UHF, so that the low impedance of D121 appears as a high impedance at the junction of D120 and the harmonic filter input. This provides a high series impedance and low shunt impedance divider between the power amplifier output and receiver input.

9.3.3 Harmonic Filter

The harmonic filter consists of components C130-C136 and L130-L132. The harmonic filter is a seven-pole Chebychev low-pass configuration, optimized for low insertion loss, with a 3 dB frequency of approximately 600 MHz and typically less than 0.8 dB insertion loss in the passband.

9.3.4 Antenna Matching Network

The harmonic filter presents a 50Ω impedance to antenna jack J140. A matching network, made up of C140-C141 and L140, is used to match the antenna impedance to the harmonic filter. This optimizes the performance of the transmitter and receiver into the impedance presented by the antenna, significantly improving the antenna's efficiency.

9.3.5 Power Control

The power control circuit is a dc-coupled amplifier whose output is the dc gate bias voltage (VGG) applied to the two stages of the RF power amplifier U110.

The output power of the transmitter is adjusted by varying the setting of the power-set DAC contained in the ASFICcmp IC (DACG, U451 pin 6). This PWR_SET voltage is applied to U150 pin 3.

Stage U150-2 compares the voltage drop across current sense resistor R150 to the voltage drop across resistor R151 caused by current flow through Q150, and adjusts its output (pin 7) to maintain equal voltages at pins 5 and 6. Thus the current flow through Q150, and hence its emitter voltage, is proportional to the current drawn by stage U110, which is in turn proportional to the transmitter output power. The emitter voltage of Q150 is applied to U150 pin 2, where it is compared to the power set voltage PWR_SET at pin 3.

The output of U150 pin 1 is divided by R110 and R111 and applied as a gate voltage to the power amplifier U110. By varying this gate voltage as needed to keep the voltages at U150 pins 2 and 3 equal, power is maintained at the desired setting. Excessive final current, for example due to antenna mismatch, causes a lowering of the voltage at U150 pin 6, an increased voltage at pin 2, and a lowering of the voltage at pin 1 and of the gate voltage VGG. This prevents damage to the final stage due to excessive current.

9.4 UHF Frequency Generation Circuitry

The frequency generation system, shown in Figure 9-3, is composed of two circuit blocks, the Fractional-N synthesizer IC U201, the VCO/Buffer IC U251, and associated circuitry. Figure 9-4 shows the peripheral interconnect and support circuitry used in the synthesizer block, and Figure 9-5 details the internal circuitry of the VCOBIC and its interconnections to the surrounding components. Refer to the schematic to identify reference designators.

The Fractional-N synthesizer is powered by regulated 5 V and 3 V provided by U310 and U330 respectively. 5 V is applied to U201 pins 13 and 30, and 3 V is applied to pins 5, 20, 34 and 36. The synthesizer in turn generates a super-filtered 4.5 V supply (VSF, from pin 28) to power U251. In addition to the VCO, the synthesizer also interfaces with the logic and ASFICcmp circuits. Programming for the synthesizer is accomplished through the microprocessor SPI_DATA_OUT,

SPI_CLK, and SYNTH_CS (chip select) lines (U409 pins 100, 1 and 47 respectively). A logic high (3 V) from U201 pin 4 indicates to the microprocessor that the synthesizer is locked.

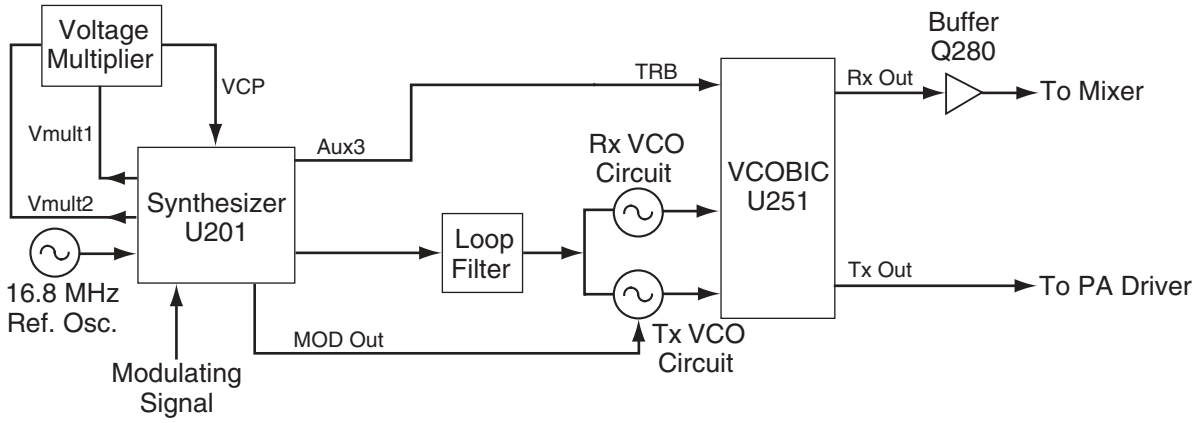

Figure 9-3. UHF Frequency Generation Unit Block Diagram

Transmit modulation from the ASFICcmp (U451 pin 40) is applied to U201 pin 10 (MOD_IN). An electronic attenuator in the ASFICcmp adjusts overall transmitter deviation by varying the audio level applied to the synthesizer IC. Internally the audio is digitized by the Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio is also routed through an internal attenuator for the purpose of balancing the low port and high port modulation and reducing the deviation by 6 dB for 12.5 kHz channels, and is available at U201 pin 41 (VCO_MOD). This audio signal is routed to the VCO's modulator.

9.4.1 Fractional-N Synthesizer

The Fractional-N synthesizer, shown in Figure 9-4, uses a 16.8 MHz crystal (Y201) to provide the reference frequency for the system. External components C201-C203, R202 and D201 are also part of the temperature-compensated oscillator circuit. The dc voltage applied to varactor D201 from U201 pin 25 is determined by a temperature-compensation algorithm within U201, and is specific to each crystal Y201, based on a unique code assigned to the crystal that identifies its temperature characteristics. Stability is better than 2.5 ppm over temperatures of -30 to 60°C. Software-programmable electronic frequency adjustment is achieved by an internal DAC which provides a frequency adjustment voltage from U201 pin 25 to varactor D201.

The synthesizer IC U201 further divides the 16.8 MHz signal to 2.1 MHz, 2.225 MHz, or 2.4 MHz for use as reference frequencies. It also provides a buffered 16.8 MHz signal at U201 pin 19 for use by the ASFICcmp.

To achieve fast locking of the synthesizer, an internal adapt charge pump provides higher current at U201 pin 45 to quickly force the synthesizer within lock range. The required frequency is then locked by the normal mode charge pump at pin 43. A loop filter (C243-C245 and R243-R245) removes noise and spurs from the steering voltage applied to the VCO varactors, with additional filtering located in the VCO circuit.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C221-C224 and D220-D221. Two 3 V square waves from U201 pins 14-15 provide the drive signals for the voltage multiplier, which generates 12.1 V at U201 pin 47. This voltage is filtered by C225-C228.

One of the auxiliary outputs of the synthesizer IC (AUX3, U201 pin 2) provides the TRB signal which determines the operating mode of the VCO, either receive or transmit.

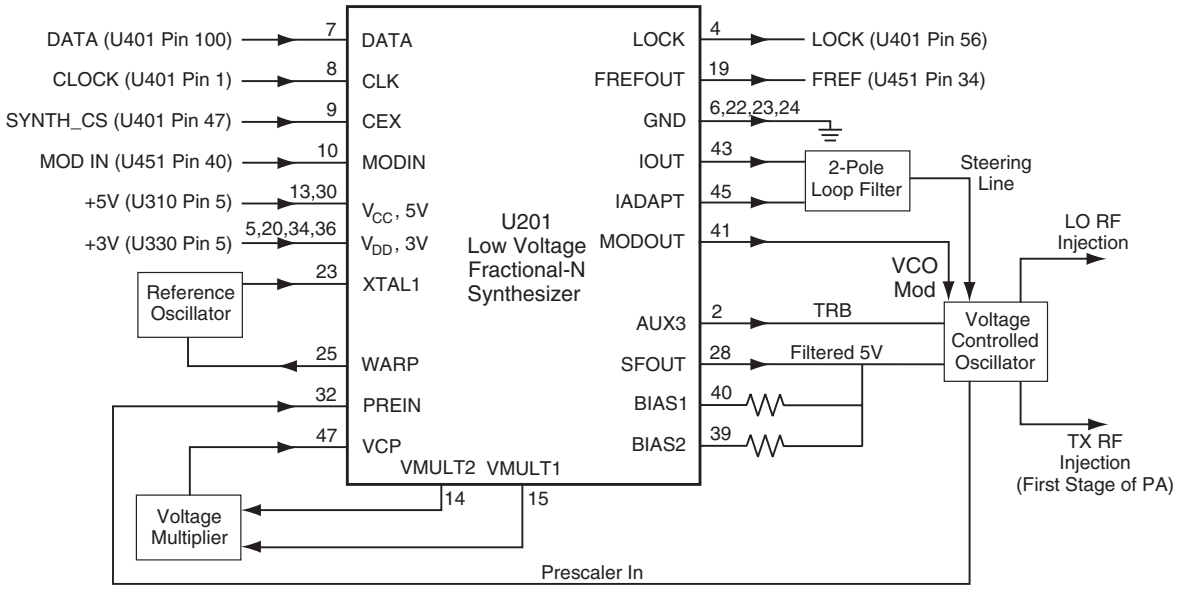

Figure 9-4. UHF Synthesizer Block Diagram

9.4.2 Voltage Controlled Oscillator (VCO)

The VCOBIC (U251), shown in Figure 9-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U251 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U251 pin 12 through a low pass filter, to the prescaler input of the synthesizer IC (U201 pin 32). After frequency comparison in the synthesizer, a resultant DC control voltage is used to steer the VCO frequency. When the PLL is locked on frequency, this voltage can vary between 3.5 V and 10 V. L251 and C252 further attenuate noise and spurs on the steering line voltage.

In the receive mode, the TRB line (U251 pin 19) is low. This activates the receive VCO and the receive buffer of U251, which operate within the range of 393.15 to 425.15 MHz. The VCO frequency is determined by tank inductor L254, C253-C257, and varactor D251. The buffered RF signal at U251 pin 8 is further amplified by Q280 and applied as RX_INJ to the low-pass injection filter in the receiver front end circuit.

In the transmit mode, U251-19 is driven high by U201 pin 2, enabling the transmit VCO and buffer. The 438-470 MHz RF signal from U251 pin 10 is applied as TX_INJ to the input of the transmitter circuit via matching network C290-C291 and L291. TX VCO frequency is determined by L264, C263-

C267, and varactor D261. High-port audio modulation from the synthesizer IC is applied as VCO_MOD to varactor D262 which modulates the transmit VCO.

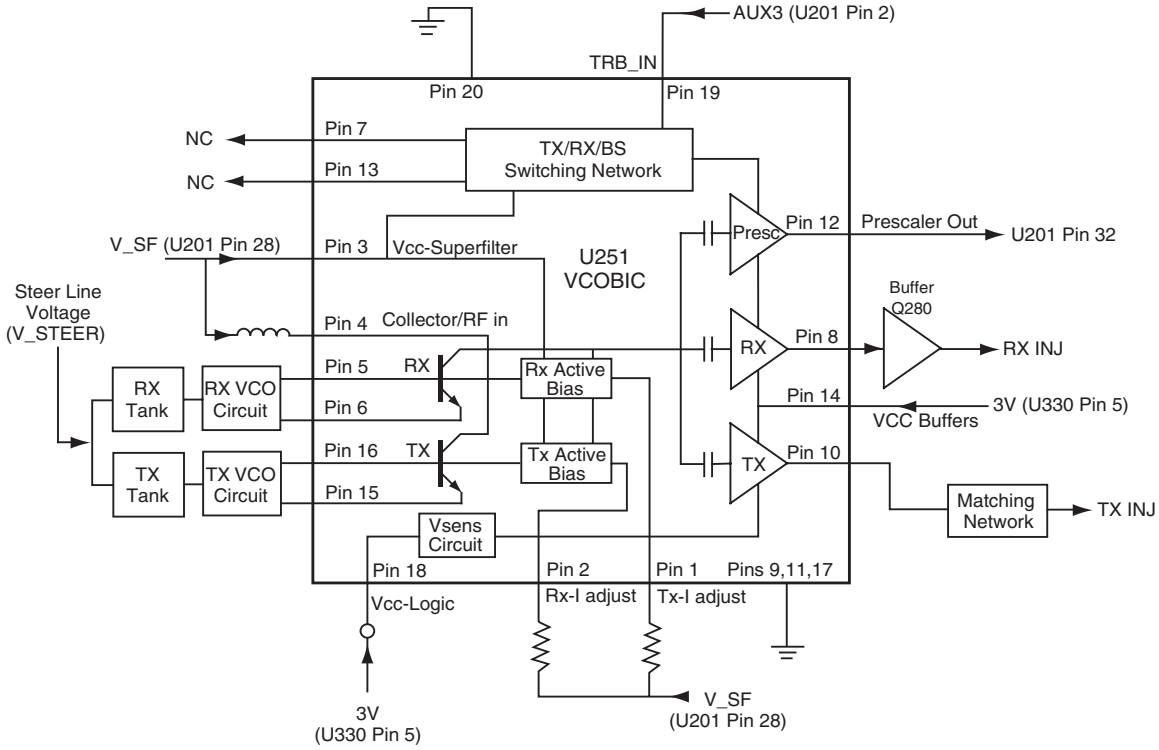

Figure 9-5. UHF VCO Block Diagram

9.5 Keypad

The keypad block diagram is shown in Figure 9-6. Pressing a key creates two distinct voltages KEYPAD_ROW and KEYPAD_COL. These voltages are sent directly to the radio's microprocessor on the main board. The microprocessor then interprets the voltage for KEYPAD_ROW and KEYPAD_COL for each key press.

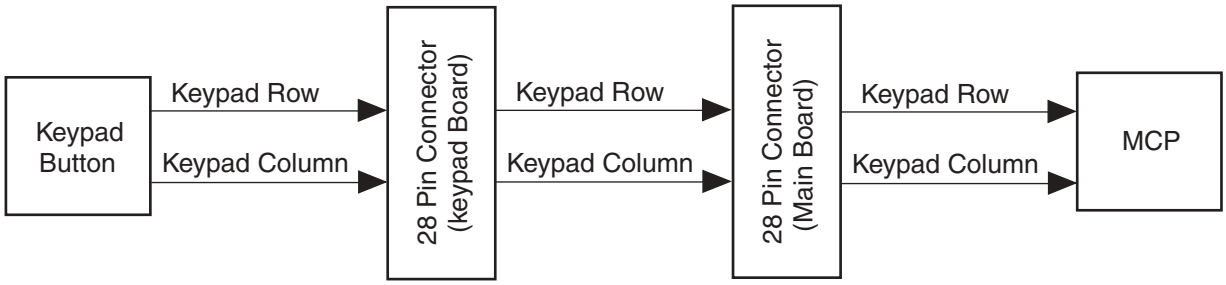

Figure 9-6. Keypad Block Diagram

Notes:

Chapter 10 465-495 MHz UHF Theory Of Operation

10.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Chapter 13 of this manual.

10.2 UHF Receiver

The UHF receiver covers the range of 465-495 MHz and provides switchable IF bandwidth for use with 20/25/30 kHz or 12.5 kHz channel spacing systems. The receiver is divided into two major blocks, as shown in Figure 10-1.

- Front End
- Back End

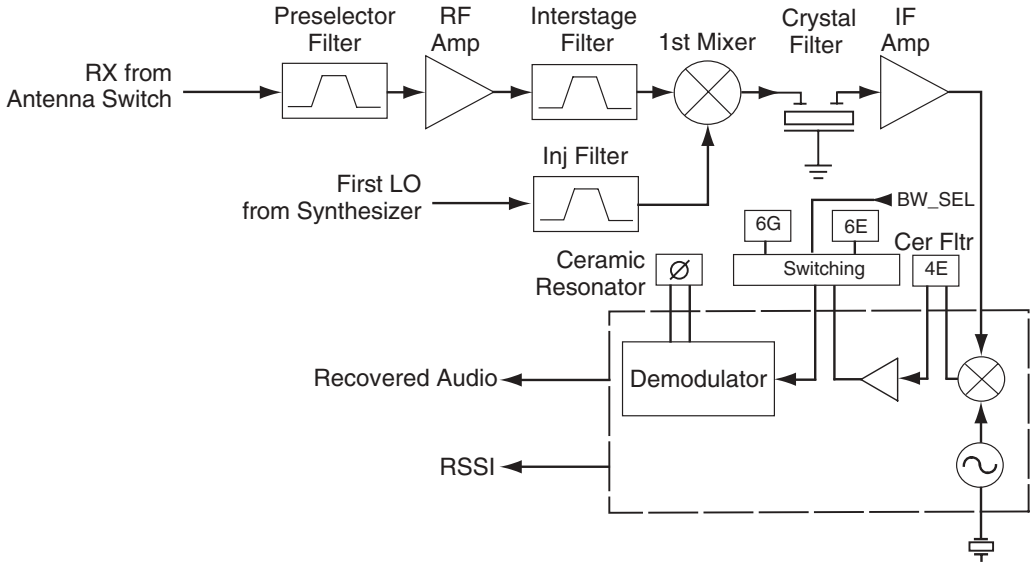

Figure 10-1. UHF Receiver Block Diagram

10.2.1 Receiver Front End

Incoming RF signals from the antenna are first routed through the harmonic filter and antenna switch, part of the transmitter circuitry, before being applied to the receiver front end. The receiver front end consists of a preselector filter, RF amplifier, an interstage filter, and a double-balanced first mixer.

The preselector filter is a fixed-tuned 3-pole Butterworth design using discrete elements (L1-L3, C1-C10, C12 and C523) in a shunt-resonator configuration. It has a 3 dB bandwidth of 68 MHz centered at 480 MHz, an insertion loss of 2 dB and image attenuation of 39 dB at 405.3 MHz. Diode CR1 protects the RF amplifier by limiting excessive RF levels. The filter bandwidth is considerably wider than the receive band, to achieve low insertion loss in a compact size. C523 provides a transmission-zero to improve image attenuation.

The output of the filter is matched to the base of RF amplifier Q21, which provides 18 dB of gain and a noise figure of 3.3 dB. A BFS505 device is used for high gain, low noise figure and reduced operating current. Operating voltage is obtained from the 5R source, which is turned off during transmit to reduce dissipation in Q21. Current mirror Q22 maintains the operating current of Q21 constant at 8 mA regardless of device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the interstage filter, a fixed-tuned 4-pole Butterworth shunt-coupled resonator design having a 3 dB bandwidth of 68 MHz centered at 480 MHz, and insertion loss of 3.3 dB. This filter yields an image rejection of 55 dB at 405.3 MHz, assisted by a transmission-zero at 300 MHz implemented by C524 for the reasons mentioned above.

The output of the interstage filter is connected to the passive double-balanced mixer consisting of components T41, T42, and CR41. This mixer has a conversion loss of 7.2 dB. Low-side injection from the frequency synthesizer is filtered by L40-L41 and C41-C45 to remove second harmonic energy that may degrade half-IF spurious rejection performance. The injection filter has a 3 dB bandwidth of 100 MHz centered at 408 MHz, and an insertion loss of 2.5 dB. The second-harmonic rejection is typically 40 dB or greater. The filtered injection signal is applied to T42 at a level of +6 dBm.

The mixer output is applied to a diplexer network (L51-L52, C51, R51) which matches the 44.85 MHz IF signal to crystal filter FL51, and terminates the mixer into 50Ω at all other frequencies.

10.2.2 Receiver Back End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL51, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of ±6.7 kHz, a maximum 20 dB bandwidth of + 12.5 kHz, and a maximum insertion loss of 3.5 dB. The output is matched to IF amplifier stage Q51 by L53 and C93. Q51 provides 16 dB of gain and a noise figure of 1.8 dB. The dc operating current is 1 mA. The output of Q51 is applied to the input of the receiver IFIC U51. Diode CR51 limits the maximum RF level applied to the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency, 44.395 MHz, is determined by Y51. The second mixer converts the 44.85 MHz high IF frequency to 455 kHz.

Additional IF selectivity is provided by two ceramic filters, FL52 (between the second mixer and IF amp) and FL53 or FL54 (between the IF amp and the limiter input). The wider filter FL53 is used for 20/25 kHz channel spacing, and the narrower filter FL54 is used for 12.5 kHz channels. When the BW_SEL line is high, the two upper diodes in packages D51 and D52 are forward biased, selecting FL53 for 20/25 kHz channels. When the BW_SEL line is low, the two lower diodes in packages D51 and D52 are forward biased, selecting FL54 for 12.5 kHz channels.

The ceramic filters have the following specifications:

	FL52	**FL53**	**FL54**
Number of Elements:	4	6	6
Insertion Loss:	4 dB	4 dB	4 dB
6 dB Bandwidth:	15 kHz	15 kHz	9 kHz
50 dB Bandwidth:	30 kHz	30 kHz	22 kHz
Stopband Rejection:	27 dB	47 dB	47 dB

Ceramic resonator Y70 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q70 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering the distortion of the recovered audio signal. The recovered audio level at the DEMOD output is 120 mV rms (25 kHz channel, 3 kHz deviation) or 60 mV rms (12.5 kHz channel, 1.5 kHz deviation). An additional RSSI output provides a DC voltage level that is proportional to RF signal level. This voltage is measured by an A/D converter contained in the microprocessor (PE4_AN4, U401 pin 63).

10.3 UHF Transmitter

The UHF transmitter covers the range of 465-495 MHz. Depending on model, the output power of the transmitter is either switchable on a per-channel basis between high power (4 watts) and low power (1 watt), or is factory preset to 2 watts. The transmitter is divided into four major blocks as shown in Figure 10-2.

- Power Amplifier
- Harmonic Filter
- Antenna Matching Network
- Power Control.

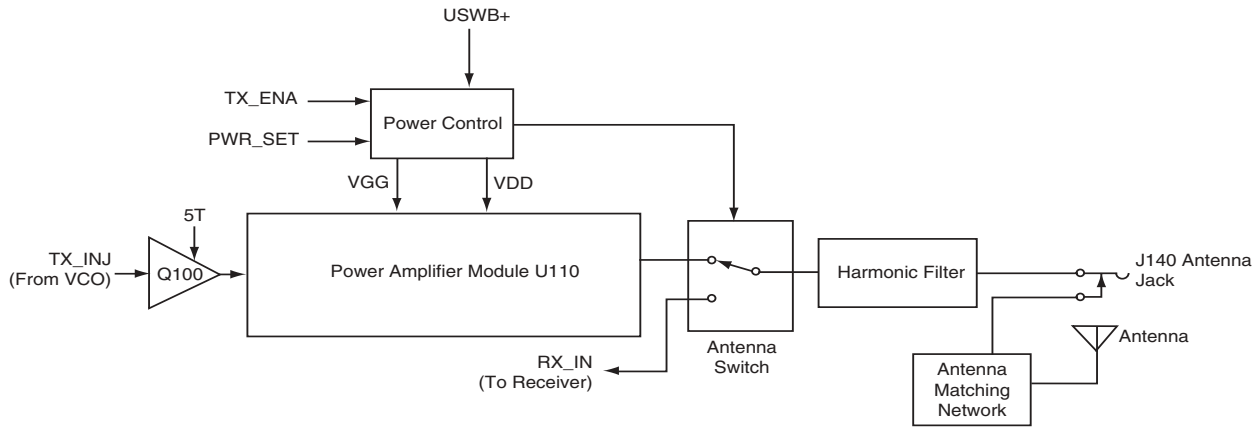

Figure 10-2. UHF Transmitter Block Diagram

10.3.1 Transmitter Power Amplifier

The transmitter power amplifier has three stages of amplification. The first stage, Q100, operates in Class A from the 5T source. It provides 17 dB of gain and an output of 50 mW. The current drain is typically 30mA. Components C105 and L103 match the output of Q100 to the 50Ω input of the module U110.

U110 is a two stage Silicon MOS FET power amplifier module. Drain voltage is obtained from UNSW B+ after being routed through current-sense resistor R150 in the power control circuit. The output power of the module is controlled by varying the DC gate bias on U110 pin 2 (VGG).

10.3.2 Antenna Switch

The antenna switch consists of two pin diodes, D120 and D121. In the receive mode, both diodes are off. Signals applied at the antenna or at jack J140 are routed, via the harmonic filter, through network C122-C124 and L121, to the receiver input. In the transmit mode, Q170 is on and TXB+ is present, forward-biasing both diodes into conduction. The diode current is 20 mA, set by R120-R121. The transmitter RF from U110 is routed through D120, and via the harmonic filter to the antenna jack. D121 conducts, shunting RF power and preventing it from reaching the receiver. L121 is selected to appear as a 1/4 wave at UHF, so that the low impedance of D121 appears as a high impedance at the junction of D120 and the harmonic filter input. This provides a high series impedance and low shunt impedance divider between the power amplifier output and receiver input.

10.3.3 Harmonic Filter

The harmonic filter consists of components C130-C136 and L130-L132. The harmonic filter is a seven-pole Chebychev low-pass configuration, optimized for low insertion loss, with a 3 dB frequency of approximately 655 MHz and typically less than 0.8 dB insertion loss in the passband.

10.3.4 Antenna Matching Network

The harmonic filter presents a 50Ω impedance to antenna jack J140. A matching network, made up of C140-C141 and L140, is used to match the antenna impedance to the harmonic filter. This optimizes the performance of the transmitter and receiver into the impedance presented by the antenna, significantly improving the antenna's efficiency.

10.3.5 Power Control

The power control circuit is a dc-coupled amplifier whose output is the dc gate bias voltage (VGG) applied to the two stages of the RF power amplifier U110.

The output power of the transmitter is adjusted by varying the setting of the power-set DAC contained in the ASFICcmp IC (DACG, U451 pin 6). This PWR_SET voltage is applied to U150 pin 3.

Stage U150-2 compares the voltage drop across current sense resistor R150 to the voltage drop across resistor R151 caused by current flow through Q150, and adjusts its output (pin 7) to maintain equal voltages at pins 5 and 6. Thus the current flow through Q150, and hence its emitter voltage, is proportional to the current drawn by stage U110, which is in turn proportional to the transmitter output power. The emitter voltage of Q150 is applied to U150 pin 2, where it is compared to the power set voltage PWR_SET at pin 3.

The output of U150 pin 1 is divided by R110 and R111 and applied as a gate voltage to the power amplifier U110. By varying this gate voltage as needed to keep the voltages at U150 pins 2 and 3 equal, power is maintained at the desired setting. Excessive final current, for example due to antenna mismatch, causes a lowering of the voltage at U150 pin 6, an increased voltage at pin 2, and a lowering of the voltage at pin 1 and of the gate voltage VGG. This prevents damage to the final stage due to excessive current.

10.4 UHF Frequency Generation Circuitry

The frequency generation system, shown in Figure 10-3, is composed of two circuit blocks, the Fractional-N synthesizer IC U201, the VCO/Buffer IC U251, and associated circuitry. Figure 10-4 shows the peripheral interconnect and support circuitry used in the synthesizer block, and Figure 10-5 details the internal circuitry of the VCOBIC and its interconnections to the surrounding components. Refer to the schematic to identify reference designators.

The Fractional-N synthesizer is powered by regulated 5 V and 3 V provided by U310 and U330 respectively. 5 V is applied to U201 pins 13 and 30, and 3 V is applied to pins 5, 20, 34 and 36. The synthesizer in turn generates a super-filtered 4.5 V supply (VSF, from pin 28) to power U251. In addition to the VCO, the synthesizer also interfaces with the logic and ASFICcmp circuits. Programming for the synthesizer is accomplished through the microprocessor SPI_DATA_OUT,

SPI_CLK, and SYNTH_CS (chip select) lines (U409 pins 100, 1 and 47 respectively). A logic high (3 V) from U201 pin 4 indicates to the microprocessor that the synthesizer is locked.

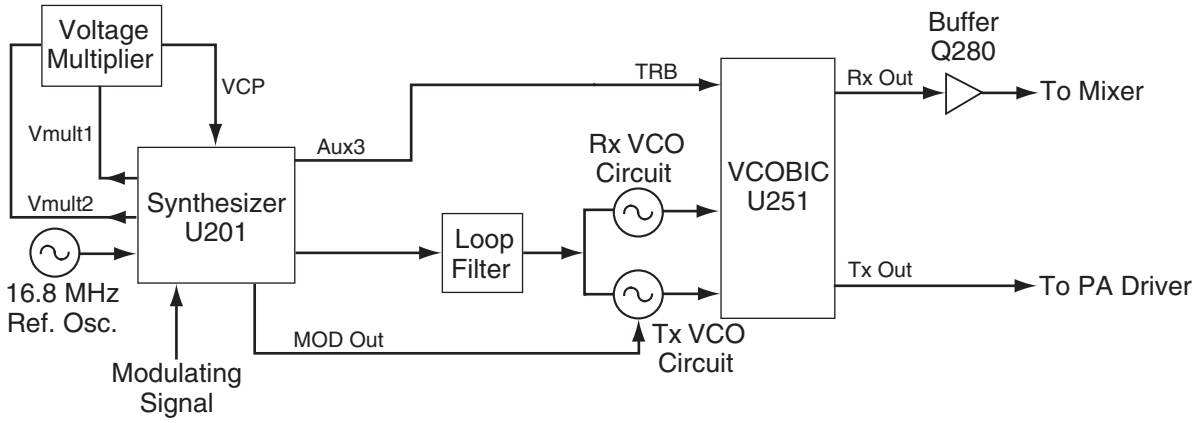

Figure 10-3. UHF Frequency Generation Unit Block Diagram

Transmit modulation from the ASFICcmp (U451 pin 40) is applied to U201 pin 10 (MOD_IN). An electronic attenuator in the ASFICcmp adjusts overall transmitter deviation by varying the audio level applied to the synthesizer IC. Internally the audio is digitized by the Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio is also routed through an internal attenuator for the purpose of balancing the low port and high port modulation and reducing the deviation by 6 dB for 12.5 kHz channels, and is available at U201 pin 41 (VCO_MOD). This audio signal is routed to the VCO's modulator.

10.4.1 Fractional-N Synthesizer

The Fractional-N synthesizer, shown in Figure 10-4, uses a 16.8 MHz crystal (Y201) to provide the reference frequency for the system. External components C201-C203, R202 and D201 are also part of the temperature-compensated oscillator circuit. The dc voltage applied to varactor D201 from U201 pin 25 is determined by a temperature-compensation algorithm within U201, and is specific to each crystal Y201, based on a unique code assigned to the crystal that identifies its temperature characteristics. Stability is better than 2.5 ppm over temperatures of -30 to 60°C. Software-programmable electronic frequency adjustment is achieved by an internal DAC which provides a frequency adjustment voltage from U201 pin 25 to varactor D201.

The synthesizer IC U201 further divides the 16.8 MHz signal to 2.1 MHz, 2.225 MHz, or 2.4 MHz for use as reference frequencies. It also provides a buffered 16.8 MHz signal at U201 pin 19 for use by the ASFICcmp.

To achieve fast locking of the synthesizer, an internal adapt charge pump provides higher current at U201 pin 45 to quickly force the synthesizer within lock range. The required frequency is then locked by the normal mode charge pump at pin 43. A loop filter (C243-C245 and R243-R245) removes noise and spurs from the steering voltage applied to the VCO varactors, with additional filtering located in the VCO circuit.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C221-C224 and D220-D221. Two 3 V square waves from U201 pins 14-15 provide the drive signals for the voltage multiplier, which generates 12.1 V at U201 pin 47. This voltage is filtered by C225-C228.

One of the auxiliary outputs of the synthesizer IC (AUX3, U201 pin 2) provides the TRB signal which determines the operating mode of the VCO, either receive or transmit.

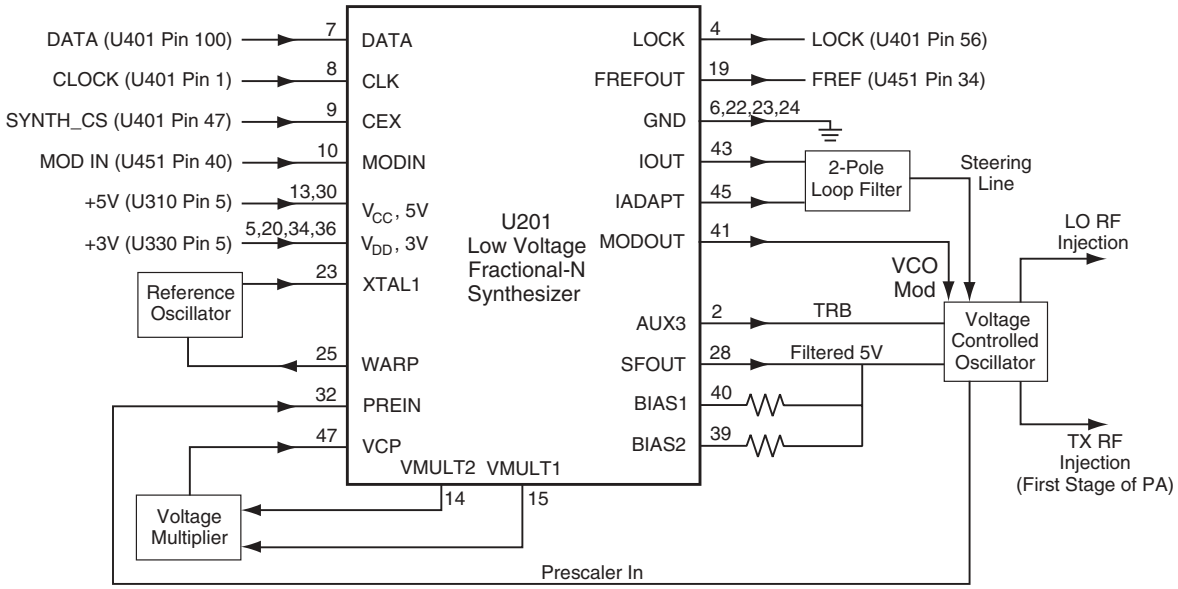

Figure 10-4. UHF Synthesizer Block Diagram

10.4.2 Voltage Controlled Oscillator (VCO)

The VCOBIC (U251), shown in Figure 10-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U251 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U251 pin 12 through a low pass filter, to the prescaler input of the synthesizer IC (U201 pin 32). After frequency comparison in the synthesizer, a resultant DC control voltage is used to steer the VCO frequency. When the PLL is locked on frequency, this voltage can vary between 3.5 V and 10 V. L251 and C252 further attenuate noise and spurs on the steering line voltage.

In the receive mode, the TRB line (U251 pin 19) is low. This activates the receive VCO and the receive buffer of U251, which operate within the range of 420.15 to 450.15 MHz. The VCO frequency is determined by tank inductor L254, C253-C257, and varactor D251. The buffered RF signal at U251 pin 8 is further amplified by Q280 and applied as RX_INJ to the low-pass injection filter in the receiver front end circuit.

In the transmit mode, U251-19 is driven high by U201 pin 2, enabling the transmit VCO and buffer. The 465-495 MHz RF signal from U251 pin 10 is applied as TX_INJ to the input of the transmitter circuit via matching network C290-C291 and L291. TX VCO frequency is determined by L264, C263-

C267, and varactor D261. High-port audio modulation from the synthesizer IC is applied as VCO_MOD to varactor D262 which modulates the transmit VCO.

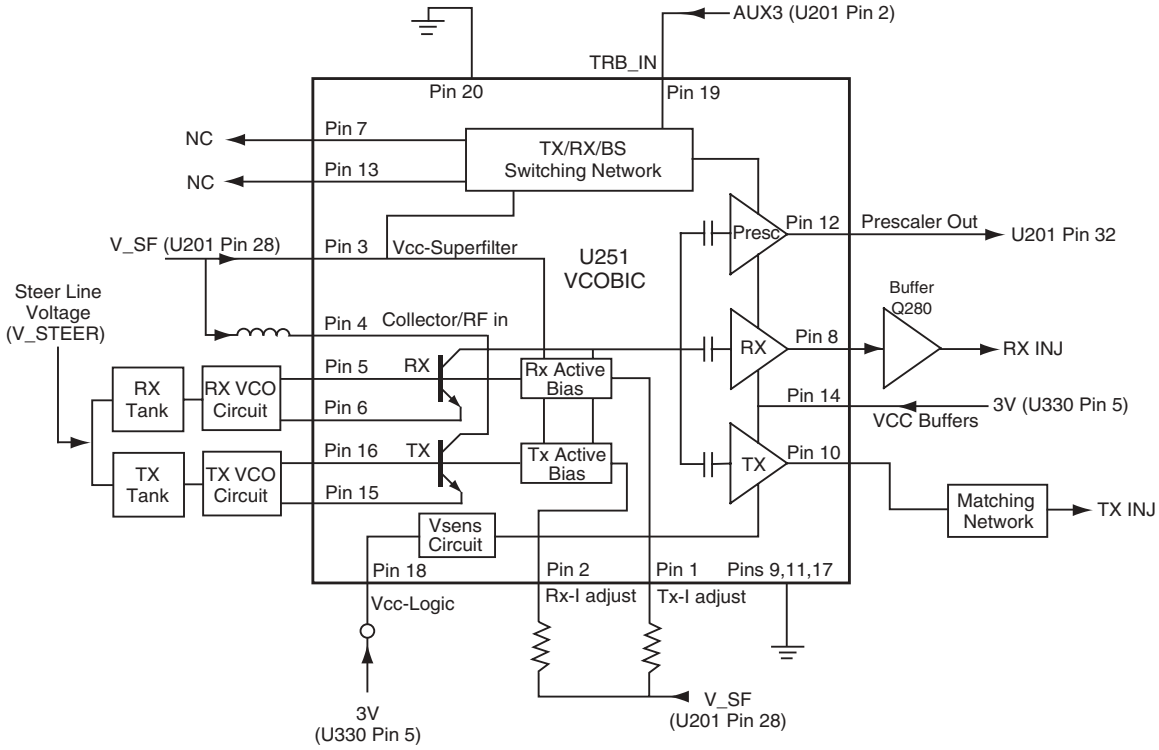

Figure 10-5. UHF VCO Block Diagram

10.5 Keypad

The keypad block diagram is shown in Figure 10-6. Pressing a key creates two distinct voltages KEYPAD_ROW and KEYPAD_COL. These voltages are sent directly to the radio's microprocessor on the main board. The microprocessor then interprets the voltage for KEYPAD_ROW and KEYPAD_COL for each key press.

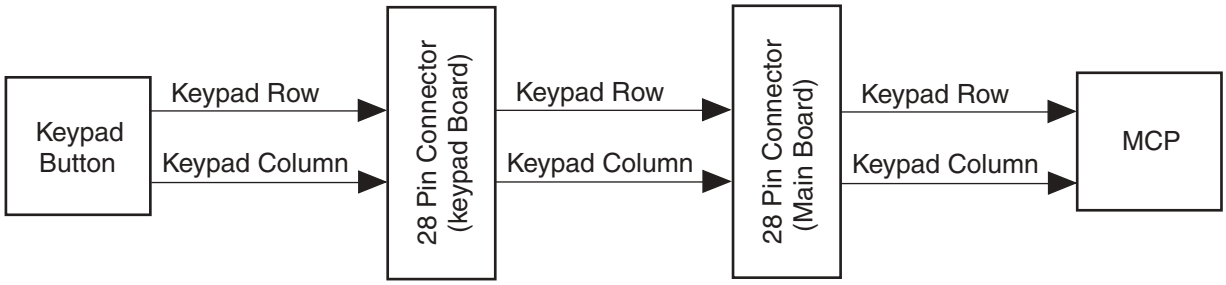

Figure 10-6. Keypad Block Diagram

Notes:

Chapter 11 490-527 MHz UHF Theory Of Operation

11.1 Introduction

This chapter provides a detailed theory of operation for the radio components. Schematic diagrams for the circuits described in the following paragraphs are located in Chapter 13 of this manual.

11.2 UHF Receiver

The UHF receiver covers the range of 490-527 MHz and provides switchable IF bandwidth for use with 20/25/30 kHz or 12.5 kHz channel spacing systems. The receiver is divided into two major blocks, as shown in Figure 11-1.

- Front End
- Back End

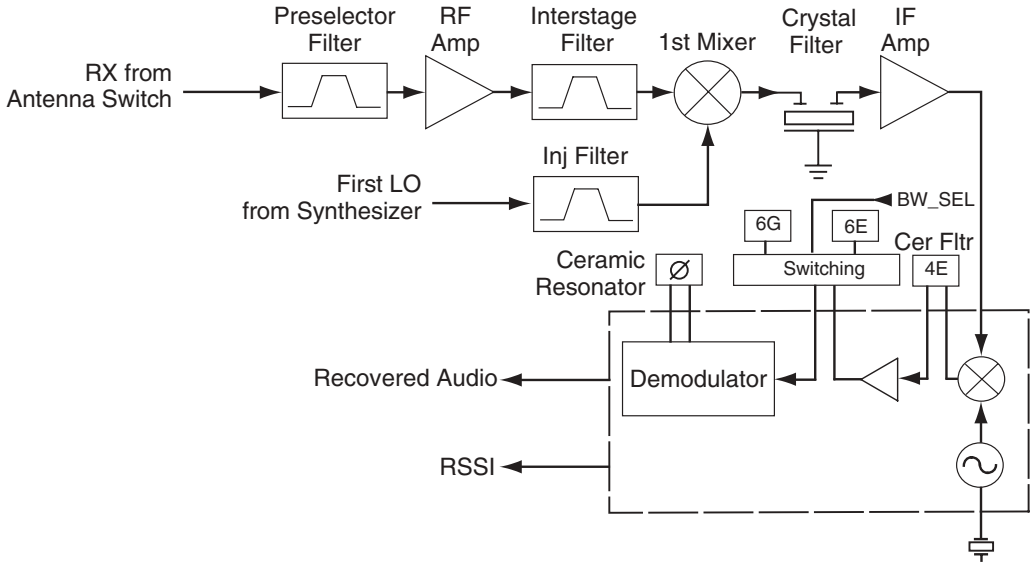

Figure 11-1. UHF Receiver Block Diagram

11.2.1 Receiver Front End

Incoming RF signals from the antenna are first routed through the harmonic filter and antenna switch, part of the transmitter circuitry, before being applied to the receiver front end. The receiver front end consists of a preselector filter, RF amplifier, an interstage filter, and a double-balanced first mixer.

The preselector filter is a fixed-tuned 3-pole Butterworth design using discrete elements (L1-L3, C1-C10, C12 and C523) in a shunt-resonator configuration. It has a 3 dB bandwidth of 68 MHz centered at 480 MHz, an insertion loss of 2 dB and image attenuation of 39 dB at 405.3 MHz. Diode CR1 protects the RF amplifier by limiting excessive RF levels. The filter bandwidth is considerably wider than the receive band, to achieve low insertion loss in a compact size. C523 provides a transmission-zero to improve image attenuation.

The output of the filter is matched to the base of RF amplifier Q21, which provides 18 dB of gain and a noise figure of 3.3 dB. A BFS505 device is used for high gain, low noise figure and reduced operating current. Operating voltage is obtained from the 5R source, which is turned off during transmit to reduce dissipation in Q21. Current mirror Q22 maintains the operating current of Q21 constant at 8 mA regardless of device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the interstage filter, a fixed-tuned 4-pole Butterworth shunt-coupled resonator design having a 3 dB bandwidth of 68 MHz centered at 480 MHz, and insertion loss of 3.3 dB. This filter yields an image rejection of 55 dB at 405.3 MHz, assisted by a transmission-zero at 300 MHz implemented by C524 for the reasons mentioned above.

The output of the interstage filter is connected to the passive double-balanced mixer consisting of components T41, T42, and CR41. This mixer has a conversion loss of 7.2 dB. Low-side injection from the frequency synthesizer is filtered by L40-L41 and C41-C45 to remove second harmonic energy that may degrade half-IF spurious rejection performance. The injection filter has a 3 dB bandwidth of 100 MHz centered at 408 MHz, and an insertion loss of 2.5 dB. The second-harmonic rejection is typically 40 dB or greater. The filtered injection signal is applied to T42 at a level of +6 dBm.

The mixer output is applied to a diplexer network (L51-L52, C51, R51) which matches the 44.85 MHz IF signal to crystal filter FL51, and terminates the mixer into 50Ω at all other frequencies.

11.2.2 Receiver Back End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL51, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of ±6.7 kHz, a maximum 20 dB bandwidth of + 12.5 kHz, and a maximum insertion loss of 3.5 dB. The output is matched to IF amplifier stage Q51 by L53 and C93. Q51 provides 16 dB of gain and a noise figure of 1.8 dB. The dc operating current is 1 mA. The output of Q51 is applied to the input of the receiver IFIC U51. Diode CR51 limits the maximum RF level applied to the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency, 44.395 MHz, is determined by Y51. The second mixer converts the 44.85 MHz high IF frequency to 455 kHz.

Additional IF selectivity is provided by two ceramic filters, FL52 (between the second mixer and IF amp) and FL53 or FL54 (between the IF amp and the limiter input). The wider filter FL53 is used for 20/25 kHz channel spacing, and the narrower filter FL54 is used for 12.5 kHz channels. When the BW_SEL line is high, the two upper diodes in packages D51 and D52 are forward biased, selecting FL53 for 20/25 kHz channels. When the BW_SEL line is low, the two lower diodes in packages D51 and D52 are forward biased, selecting FL54 for 12.5 kHz channels.

The ceramic filters have the following specifications:

	FL52	**FL53**	**FL54**
Number of Elements:	4	6	6
Insertion Loss:	4 dB	4 dB	4 dB
6 dB Bandwidth:	15 kHz	15 kHz	9 kHz
50 dB Bandwidth:	30 kHz	30 kHz	22 kHz
Stopband Rejection:	27 dB	47 dB	47 dB

Ceramic resonator Y70 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q70 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering the distortion of the recovered audio signal. The recovered audio level at the DEMOD output is 120 mV rms (25 kHz channel, 3 kHz deviation) or 60 mV rms (12.5 kHz channel, 1.5 kHz deviation). An additional RSSI output provides a DC voltage level that is proportional to RF signal level. This voltage is measured by an A/D converter contained in the microprocessor (PE4_AN4, U401 pin 63).

11.3 UHF Transmitter

The UHF transmitter covers the range of 490-527 MHz. Depending on model, the output power of the transmitter is either switchable on a per-channel basis between high power (4 watts) and low power (1 watt), or is factory preset to 2 watts. The transmitter is divided into four major blocks as shown in Figure 11-2.

- Power Amplifier
- Harmonic Filter
- Antenna Matching Network
- Power Control.

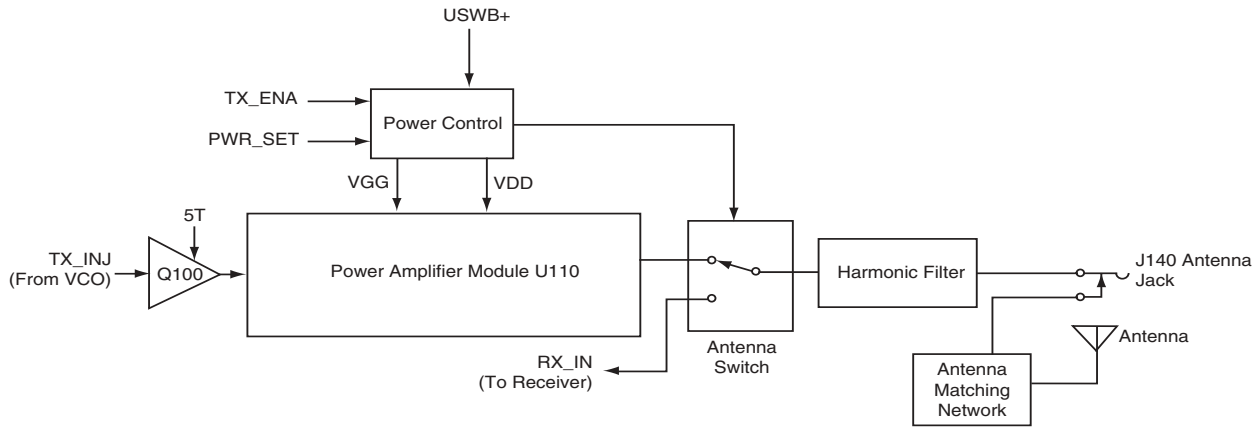

Figure 11-2. UHF Transmitter Block Diagram

11.3.1 Transmitter Power Amplifier

The transmitter power amplifier has three stages of amplification. The first stage, Q100, operates in Class A from the 5T source. It provides 17 dB of gain and an output of 50 mW. The current drain is typically 30mA. Components C105 and L103 match the output of Q100 to the 50Ω input of the module U110.

U110 is a two stage Silicon MOS FET power amplifier module. Drain voltage is obtained from UNSW B+ after being routed through current-sense resistor R150 in the power control circuit. The output power of the module is controlled by varying the DC gate bias on U110 pin 2 (VGG).

11.3.2 Antenna Switch

The antenna switch consists of two pin diodes, D120 and D121. In the receive mode, both diodes are off. Signals applied at the antenna or at jack J140 are routed, via the harmonic filter, through network C122-C124 and L121, to the receiver input. In the transmit mode, Q170 is on and TXB+ is present, forward-biasing both diodes into conduction. The diode current is 20 mA, set by R120-R121. The transmitter RF from U110 is routed through D120, and via the harmonic filter to the antenna jack. D121 conducts, shunting RF power and preventing it from reaching the receiver. L121 is selected to appear as a 1/4 wave at UHF, so that the low impedance of D121 appears as a high impedance at the junction of D120 and the harmonic filter input. This provides a high series impedance and low shunt impedance divider between the power amplifier output and receiver input.

11.3.3 Harmonic Filter

The harmonic filter consists of components C130-C136 and L130-L132. The harmonic filter is a seven-pole Chebychev low-pass configuration, optimized for low insertion loss, with a 3 dB frequency of approximately 655 MHz and typically less than 0.8 dB insertion loss in the passband.

11.3.4 Antenna Matching Network

The harmonic filter presents a 50Ω impedance to antenna jack J140. A matching network, made up of C140-C141 and L140, is used to match the antenna impedance to the harmonic filter. This optimizes the performance of the transmitter and receiver into the impedance presented by the antenna, significantly improving the antenna's efficiency.

11.3.5 Power Control

The power control circuit is a dc-coupled amplifier whose output is the dc gate bias voltage (VGG) applied to the two stages of the RF power amplifier U110.

The output power of the transmitter is adjusted by varying the setting of the power-set DAC contained in the ASFICcmp IC (DACG, U451 pin 6). This PWR_SET voltage is applied to U150 pin 3.

Stage U150-2 compares the voltage drop across current sense resistor R150 to the voltage drop across resistor R151 caused by current flow through Q150, and adjusts its output (pin 7) to maintain equal voltages at pins 5 and 6. Thus the current flow through Q150, and hence its emitter voltage, is proportional to the current drawn by stage U110, which is in turn proportional to the transmitter output power. The emitter voltage of Q150 is applied to U150 pin 2, where it is compared to the power set voltage PWR_SET at pin 3.

The output of U150 pin 1 is divided by R110 and R111 and applied as a gate voltage to the power amplifier U110. By varying this gate voltage as needed to keep the voltages at U150 pins 2 and 3 equal, power is maintained at the desired setting. Excessive final current, for example due to antenna mismatch, causes a lowering of the voltage at U150 pin 6, an increased voltage at pin 2, and a lowering of the voltage at pin 1 and of the gate voltage VGG. This prevents damage to the final stage due to excessive current.

11.4 UHF Frequency Generation Circuitry

The frequency generation system, shown in Figure 11-3, is composed of two circuit blocks, the Fractional-N synthesizer IC U201, the VCO/Buffer IC U251, and associated circuitry. Figure 11-4 shows the peripheral interconnect and support circuitry used in the synthesizer block, and Figure 11-5 details the internal circuitry of the VCOBIC and its interconnections to the surrounding components. Refer to the schematic to identify reference designators.

The Fractional-N synthesizer is powered by regulated 5 V and 3 V provided by U310 and U330 respectively. 5 V is applied to U201 pins 13 and 30, and 3 V is applied to pins 5, 20, 34 and 36. The synthesizer in turn generates a super-filtered 4.5 V supply (VSF, from pin 28) to power U251. In addition to the VCO, the synthesizer also interfaces with the logic and ASFICcmp circuits. Programming for the synthesizer is accomplished through the microprocessor SPI_DATA_OUT,

SPI_CLK, and SYNTH_CS (chip select) lines (U409 pins 100, 1 and 47 respectively). A logic high (3 V) from U201 pin 4 indicates to the microprocessor that the synthesizer is locked.

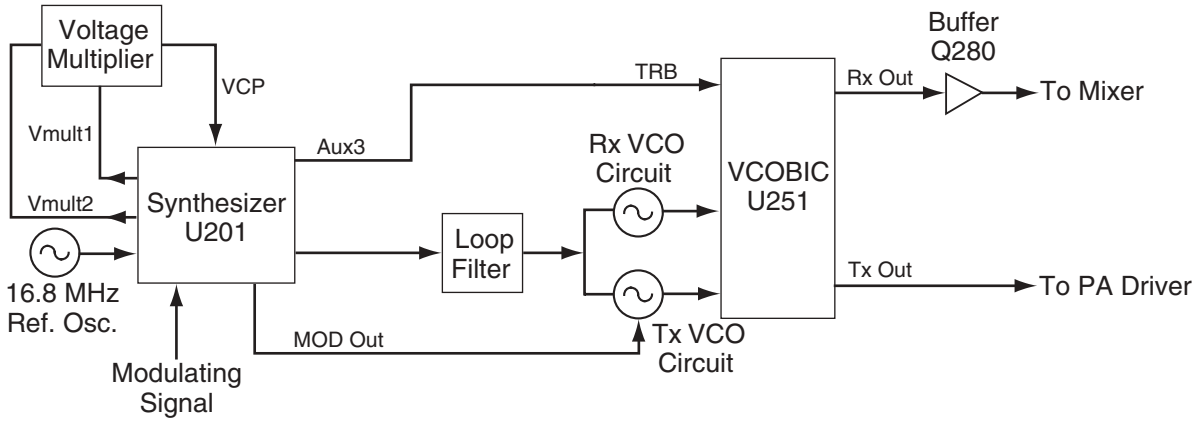

Figure 11-3. UHF Frequency Generation Unit Block Diagram

Transmit modulation from the ASFICcmp (U451 pin 40) is applied to U201 pin 10 (MOD_IN). An electronic attenuator in the ASFICcmp adjusts overall transmitter deviation by varying the audio level applied to the synthesizer IC. Internally the audio is digitized by the Fractional-N synthesizer and applied to the loop divider to provide the low-port modulation. The audio is also routed through an internal attenuator for the purpose of balancing the low port and high port modulation and reducing the deviation by 6 dB for 12.5 kHz channels, and is available at U201 pin 41 (VCO_MOD). This audio signal is routed to the VCO's modulator.

11.4.1 Fractional-N Synthesizer

The Fractional-N synthesizer, shown in Figure 11-4, uses a 16.8 MHz crystal (Y201) to provide the reference frequency for the system. External components C201-C203, R202 and D201 are also part of the temperature-compensated oscillator circuit. The dc voltage applied to varactor D201 from U201 pin 25 is determined by a temperature-compensation algorithm within U201, and is specific to each crystal Y201, based on a unique code assigned to the crystal that identifies its temperature characteristics. Stability is better than 2.5 ppm over temperatures of -30 to 60°C. Software-programmable electronic frequency adjustment is achieved by an internal DAC which provides a frequency adjustment voltage from U201 pin 25 to varactor D201.

The synthesizer IC U201 further divides the 16.8 MHz signal to 2.1 MHz, 2.225 MHz, or 2.4 MHz for use as reference frequencies. It also provides a buffered 16.8 MHz signal at U201 pin 19 for use by the ASFICcmp.

To achieve fast locking of the synthesizer, an internal adapt charge pump provides higher current at U201 pin 45 to quickly force the synthesizer within lock range. The required frequency is then locked by the normal mode charge pump at pin 43. A loop filter (C243-C245 and R243-R245) removes noise and spurs from the steering voltage applied to the VCO varactors, with additional filtering located in the VCO circuit.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C221-C224 and D220-D221. Two 3 V square waves from U201 pins 14-15 provide the drive signals for the voltage multiplier, which generates 12.1 V at U201 pin 47. This voltage is filtered by C225-C228.

One of the auxiliary outputs of the synthesizer IC (AUX3, U201 pin 2) provides the TRB signal which determines the operating mode of the VCO, either receive or transmit.

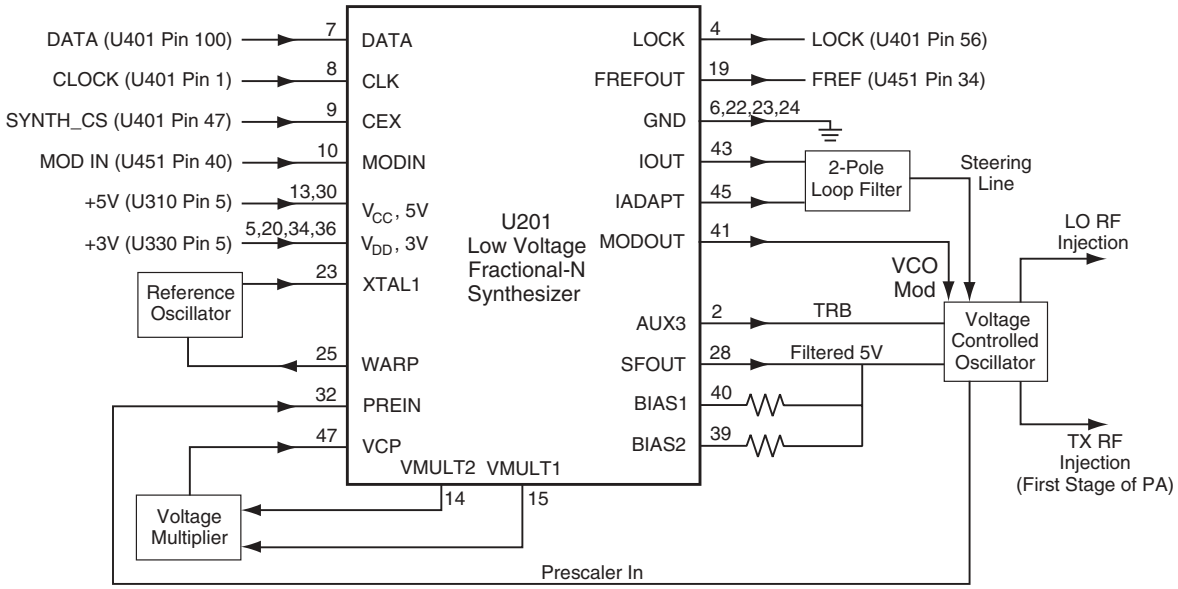

Figure 11-4. UHF Synthesizer Block Diagram

11.4.2 Voltage Controlled Oscillator (VCO)

The VCOBIC (U251), shown in Figure 11-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U251 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U251 pin 12 through a low pass filter, to the prescaler input of the synthesizer IC (U201 pin 32). After frequency comparison in the synthesizer, a resultant DC control voltage is used to steer the VCO frequency. When the PLL is locked on frequency, this voltage can vary between 3.5 V and 10 V. L251 and C252 further attenuate noise and spurs on the steering line voltage.

In the receive mode, the TRB line (U251 pin 19) is low. This activates the receive VCO and the receive buffer of U251, which operate within the range of 420.15 to 450.15 MHz. The VCO frequency is determined by tank inductor L254, C253-C257, and varactor D251. The buffered RF signal at U251 pin 8 is further amplified by Q280 and applied as RX_INJ to the low-pass injection filter in the receiver front end circuit.

In the transmit mode, U251-19 is driven high by U201 pin 2, enabling the transmit VCO and buffer. The 490-527 MHz RF signal from U251 pin 10 is applied as TX_INJ to the input of the transmitter circuit via matching network C290-C291 and L291. TX VCO frequency is determined by L264, C263-

C267, and varactor D261. High-port audio modulation from the synthesizer IC is applied as VCO_MOD to varactor D262 which modulates the transmit VCO.

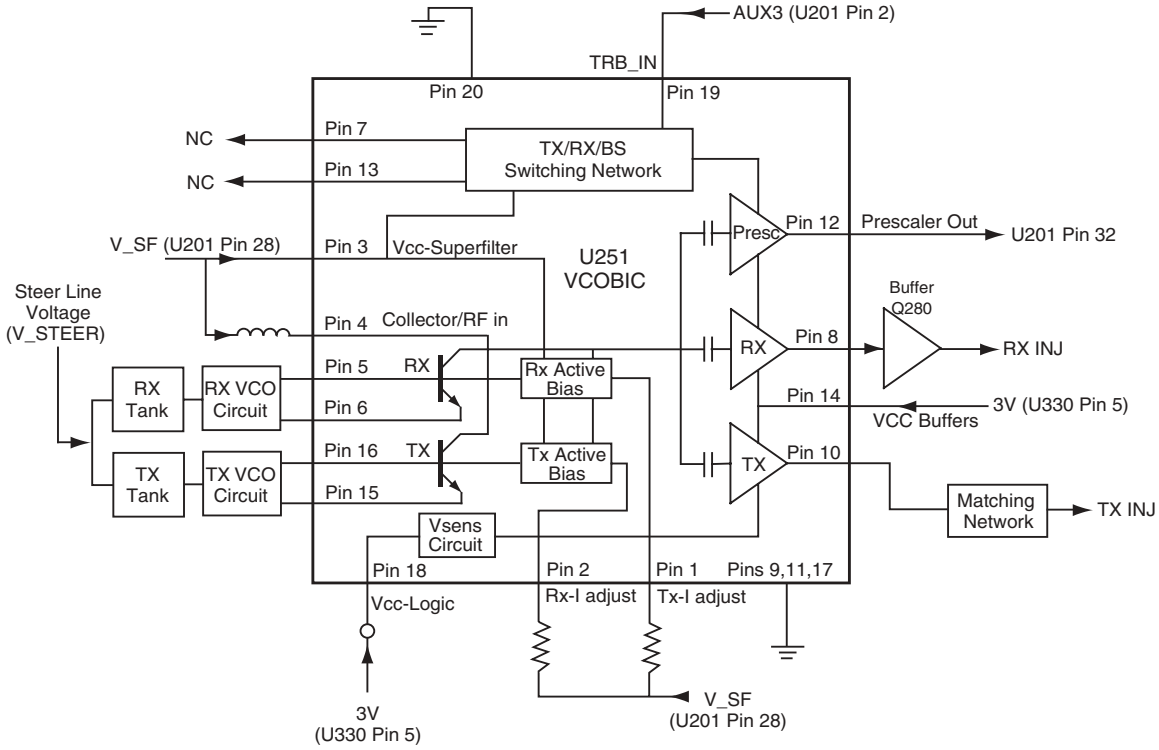

Figure 11-5. UHF VCO Block Diagram

11.5 Keypad

The keypad block diagram is shown in Figure 11-6. Pressing a key creates two distinct voltages KEYPAD_ROW and KEYPAD_COL. These voltages are sent directly to the radio's microprocessor on the main board. The microprocessor then interprets the voltage for KEYPAD_ROW and KEYPAD_COL for each key press.

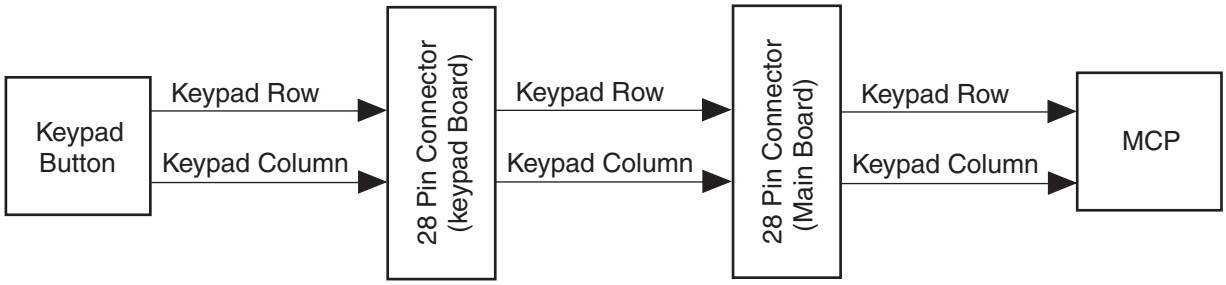

Figure 11-6. Keypad Block Diagram

Notes:

Chapter 12 UHF Troubleshooting Tables

12.1 Troubleshooting Table for Receiver

Table 12-1. Troubleshooting Table for Receiver

Symptom	Possible Causes	Procedure	Corrective Action
Radio Dead (no turn-on beep, no LED indication)	1. Battery dead or defective.	Substitute known good battery or battery eliminator.	Charge or replace battery.
	2. Defective battery contacts.	Inspect battery contacts for corrosion or bent terminals.	Clean/repair/replace J301.
	3. Blown fuse	Check voltage on each side of fuse. If blown, 0 VDC after fuse.	Check for short on output, check D301, VR301, troubleshoot/repair as needed, replace fuse.
	4. DC switching fault	Verify battery voltage present at S444 pin 5 when radio is on. Verify Q494-1 is at least 1V dc, Q494-6 is ~0.1V dc, Q493-3 is at Vbatt.	Check/replace on-off-volume control S444. Troubleshoot/replace Q493/4.
	5. Microprocessor not starting up.	Verify clock input to U401-90 (EXTAL) is 7.3975 MHz using high impedance probe. If clock is 3.8MHz, check for shorts on U401 pins. Connect RIB to verify communication via CPS. Verify U401-94 (RESET) is high.	Verify 16.8 MHz signal at U451-34. If OK, troubleshoot/replace U451. If not present, troubleshoot U201 Synthesizer. Reprogram/reflash as needed. If RESET is Low, troubleshoot regulator U320. Check for shorts at U401 pins. Replace U401. Reprogram as needed.
	6. Regulator fault	Verify U310-5 is 5V dc, U320-5 is 3.3V dc, U330-5 is 3V dc.	Check for shorts on outputs, troubleshoot/repair as needed, replace faulty regulator.

Table 12-1. Troubleshooting Table for Receiver (Continued)

Symptom	Possible Causes	Procedure	Corrective Action
No Audio	1. Synthesizer out of lock	Verify U201-4 is at 3V dc.	Troubleshoot synthesizer/VCO circuits.
	2. Defective IFIC	Verify audio is present at U51-8.	Check Q70, Y70, U51.
	3. RX audio buffer fault	Verify audio is present at U451-2.	Check U510 and associated parts.
	4. ASFIC fault	Verify audio is present at U451-41. Verify U451-14 is high.	Check squelch setting, PL/DPL programming. Troubleshoot/ replace U451.
	5. Audio PA fault	Verify U490-1 is <0.2V dc. Verify audio is present at U490-5 and 8.	Check Q490. Check/replace U490.
	6. Defective speaker	Verify audio is present at speaker terminals.	If not, check continuity of J471-2 and 3. Check J491. If yes, replace speaker.
No Receive (squelch noise present)	1. No first injection	Check that RF level at T42-6 is approx +6 dBm. Check that RF level at U251-8 is at least -8 dBm.	Check injection filter C40-44, L40-41. If yes, check Q280 and associated parts. If no, check U251 and components on pins 5 and 6.
	2. No 5R source.	Verify U401-49 is high in RX. Verify Q311 gate is 0V dc in RX Verify Q311 drain is 5V dc in RX.	Check/replace U401 Check/replace Q313. Check for shorts, check/replace Q311.
	3. Harmonic filter or antenna switch fault	Apply on-channel 100 mV RF signal at antenna port. Verify RF level at jct. C1/C2 per schematic.	Check TX harmonic filter, D120-121. Should be 0V dc on D120-121.
	4. Back end fault	Apply on-channel 100 mV RF signal at antenna port. Measure RF levels from FL51 through U51.	Check components prior to loss-of-signal point.
	5. No second injection	Measure RF level at U51-3, verify approx. 280 mV rms.	If dc voltages at U51-3 and 4 are OK, check Y51 and associated parts. If not replace U51.

12.2 Troubleshooting Table for Synthesizer

Table 12-2. Troubleshooting Table for Synthesizer

Symptom	Possible Causes	Procedure	Corrective Action
Synthesizer Out of Lock (RX mode only)	1. VCO fault	Verify oscillator is working, check RF level at U251-10 per schematic. Check dc voltages at U251 pin 2 through 6 and 10 per Table 12-4. Verify steering line voltage is between ~3V and 10V.	Check VCO tank components connected to U251-5 and 6. Check for shorts/opens, replace U251. Check D251 and associated components.
	2. Synthesizer fault	Verify TRB line (from U201-2 to U251-19) is low in RX mode	Check for shorts, check U201 voltages per Table 12-4, replace U201 if incorrect.
	3. Programming fault	Verify RX channel programming is correct.	Re-program if necessary.
Synthesizer Out of Lock (TX mode only)	1. VCO fault	Verify oscillator is working, check RF level at U251-10 per schematic. Check dc voltages at U251 pins 1,3,4,10,15,16 per Table 12-4. Verify steering line voltage is between ~3V and 10V.	Check VCO tank components connected to U251-15 and 16. Check for shorts/opens, replace U251. Check D261 and associated components.
	2. Synthesizer fault	Verify TRB line (U201-2 to U251-19) is high (3V) in TX mode	Check for shorts, check U201 voltages per Table 12-4, replace U201 if incorrect.
	3. Programming fault	Verify TX channel programming is correct.	Re-program if necessary.
Synthesizer Out of Lock (RX and TX modes)	1. VCO fault	Check that RF level at U251-12 is at least 150 mV (VHF) or -12 to -20 dBm (UHF)	If low/missing, check L276, C276-7, R276.
	2. Synthesizer fault	Check that RF level at U201-32 is at least 150 mV (VHF) or -12 to -20 dBm (UHF). Verify steering line voltage is between ~3V and 10V.	If correct, check/replace U201. If incorrect, check R248 and C241. Check loop filter components R243-5 and C243-5.
	3. DC voltage fault	Verify 4.5V dc at U201-28. Verify 12.1V dc at U201-47	Check C231-233, etc., for shorts. If OK check/replace U201. Check for 3V 1.05 MHz sq waves at U201-14 and 15. Check C218-228, D220-221.
	4. Programming fault	Verify channel programming is correct.	Re-program if necessary.

12.3 Troubleshooting Table for Transmitter

Table 12-3. Troubleshooting Table for Transmitter

Symptom	Possible Causes	Procedure	Corrective Action
No Transmit (no TX LED indication)	1. PTT switch defective.	Verify U401-71 goes low when PTT is pressed.	Replace PTT switch S441.
	2. EXT MIC PTT fault	Verify U401-72 goes low when J471-4 is grounded.	Check/replace Q470, L471 etc.
No Transmit (TX LED indication OK)	1. Synthesizer out of lock	Refer to Table 12-2.	Refer to Table 12-2.
	2. No TX_ENABLE	Verify U401-50 is high when pin 71 or 72 is low.	Check/replace U401.
	3. TX DC switch fault	Verify Q171-C is 0V in TX. Verify Q170-C is at Vbatt in TX.	Replace Q171. Check for shorts, replace Q170.
	4. Power control fault	Check Q150 and U150 dc voltages per schematic and Table 12-4.	Repair/replace defective components
	5. No TX injection	Check that RF level at jct. R100/R101 per schematic.	Check U251, L291-292, C290-291.
	6. No 5T source	Verify Q312 gate is 0V dc in TX Verify Q312 drain is 5V dc in TX.	Check/replace Q313. Check for shorts, check/replace Q312.
	7. TX gain stage failure	Check RF levels at Q100 and U110 per schematic.	Troubleshoot Q100/U110 and associated circuitry.
	8. Antenna switch failure	Verify dc voltage at jct. R122/L120 is approx 1.5V.	Check/replace D120-121, L120-121, R120-122, etc.
Low Power	1. Low TX injection	Check that RF level at jct. R100/R101 per schematic.	Check U251, L291-292, C290-291.
	2. Low gain in TX stage	Verify dc voltage at Q100-E is ~1.3V (VHF) or ~0.5V (UHF). Verify that RF level at U110-1 is approx. 1V (VHF) or 1.6V (UHF).	Verify 5T voltage is correct. Troubleshoot Q100 circuitry. Troubleshoot Q100 circuitry. Check/replace Q100.
	3. Incorrect control voltage	Verify that the dc voltage at PWR_SET (R162) is approx 1.8V dc (at 1 watt) to 2.6V dc (at 4-5 watts). Verify that the dc voltage at U110-2 is approx 2-3V dc (at 1 watt) to 3-4V dc (at 4-5 watts). (See schematic.)	Check programming. Troubleshoot controller circuitry. Check/replace U451. Troubleshoot U150, Q150 and associated circuitry.
	4. Antenna switch defect	Verify dc voltage at jct. R122/L120 (VHF) or R121/L120 (UHF) is approx 1.7V. *Note: Do not attempt to measure RF or DC voltages at the diodes. Damage to test equipment may occur.*	Check/replace D120-121, L120-121, R120-122, etc.
	5. Harmonic filter defect	Visually inspect components C130-137, L130-132. Check dc continuity of L130-132 *in RX mode only.*	Repair/replace if necessary.

Table 12-3. Troubleshooting Table for Transmitter (Continued)

Symptom	Possible Causes	Procedure	Corrective Action
Poor TX range, conducted power OK	1. RF test jack defective	Verify continuity of J140 pins 3 and 4 *in RX mode only.*	Replace J140.
	2. Antenna matching network fault	Visually inspect components C140-141, L140 or L141. Check dc continuity of L140 or L141*in RX mode only.*	Repair/replace if necessary.
	3. Defective or wrong antenna	Verify correct antenna is installed. Try another antenna.	Replace antenna.
No internal mic audio (EXT MIC audio OK)	1. Mic bias fault	Verify U451-35 is low when side PTT is pressed. Verify Q470-6 is high when side PTT button is pressed.	Check/replace U451. Check/replace R474, R476, and Q470.
	2. Defective mic	Verify approx 1.8V dc across cartridge when side PTT button is pressed. Verify audio present (~10 mV rms) when speaking into mic.	Check mic connector and R478. Replace mic cartridge.
	3. Defective mic jack	Verify continuity between J471 pins 4 and 5.	Replace J471.
No EXT MIC audio	1. Mic bias fault	Verify approx 1.8V dc across EXT MIC cartridge in TX mode. Verify audio present (~10 mV rms) when speaking into mic.	Check Q470. R475, R477, L471. Check VR473, VR475, D470 for shorts.
	2. Audio path fault	Verify mic audio present (~10 mV rms) at U451-46. Verify amplified mic audio present (~200 mV rms) at U451-40.	Check L471, C470. Check/replace U451.
	3. Defective audio accessory	Try another accessory.	Replace defective accessory.

12.4 Troubleshooting Table for Board and IC Signals

Table 12-4. Troubleshooting Table for Board and IC Signals

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U51 IFIC	1	RF input 44.85 MHz	1.20	
	2	RF input decoupling	1.20	
	3	2nd LO osc output	4.02	
	4	2nd LO osc input	4.60	
	5	RSSI output	0.74	(no received signal)
	6	Vcc	4.70	
	7	Audio feedback	0.89	
	8	Audio output	1.44	DEMOD to stage U510
	9	RSSI feedback	0.74	(no received signal)
	10	Quad detector input	2.22	
	11	Limiter output	1.25	
	12	Limiter decoupling 2	1.30	
	13	Limiter decoupling 1	1.30	
	14	Limiter input	1.28	
	15	Ground	GND	
	16	IF amp output	1.22	
	17	IF amp decoupling 2	1.26	
	18	IF amp input	1.26	
	19	IF amp decoupling 1	1.26	
	20	2nd mixer output	3.09	
U52 BW Select Switch	1	Inverter 1 input	0	(25 kHz mode)
	2	Inverter 2 output	0	(25 kHz mode)
	3	Inverter 3 input (NU)	GND	
	4	Ground	GND	
	5	Inverter 3 output (NU)	4.96	
	6	Inverter 2 input	3.00	(25 kHz mode)
	7	Inverter 1 output	4.95	(25 kHz mode)
	8	Vcc	4.96	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U110 RF Power Amp	1	RF input	0	(TX mode)
	2	Vgg (gate bias)	2.65 (typ)	(TX mode) (4.25V typ at VHF)
	3	Vdd	6.59	(TX mode)
	4	RF output	--	Do not measure
	5	Ground	GND	
U150 Dual Opamp	1	Unit 1 output	4.20 (typ)	(TX mode) (5.8V typ at VHF)
	2	Unit 1 (-) input	2.39 (typ)	(TX mode)
	3	Unit 1 (+) input	2.39 (typ)	(TX mode)
	4	Ground	GND	
	5	Unit 2 (+) input	3.30 (typ)	(TX mode)
	6	Unit 2 (-) input	3.35 (typ)	(TX mode)
	7	Unit 2 output	2.23 (typ)	(TX mode)
	8	Vcc	6.79	(TX mode)
U201 Freq Synthesizer	1	AUX2 output (NU)	0	
	2	AUX3 output (TRB)	0.03	To U251-19 (RX mode)
	3	AUX4 output (NU)	0	
	4	Lock detect output	2.98	To U401-56
	5	PD Vdd	2.98	
	6	Digital ground	GND	
	7	Serial data input	3.23	
	8	Serial clock input	0	
	9	Synth chip select	3.23	From U401-47
	10	Modulation input	1.50	From U451-40
	11	VMULT4 (NU)	2.98	
	12	VMULT3 (NU)	0	
	13	VRO	4.96	
	14	VMULT2	1.49	
	15	VMULT1	1.49	
	16	INDMULT (NU)	0	
	17	NC1	0	
	18	Ref select (NU)	0	
	19	Buffered 16.8 MHz out	1.54	
	20	Analog Vdd	3.00	
	21	V bypass (NU)	1.55	
	22	Analog ground	GND	
	23	Ref osc XTAL1	2.07	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U201 Freq Synthesizer	24	Ref osc XTAL2	0	
	25	Ref osc warp output	3.00	
	26	Superfilter cap	4.48	
	27	Superfilter base (NU)	3.76	
	28	Superfilter output	4.52	
	29	NC2	0	
	30	Superfilter input	4.96	
	31	NC3	0	
	32	Prescaler input	1.97	
	33	Prescaler ground	GND	
	34	Prescaler Vdd	2.99	
	35	Prescaler Vref (NU)	1.97	
	36	Digital Vdd	2.99	
	37	TEST1 (NU)	0.01	
	38	TEST2 (NU)	0	
	39	Bias 2	3.38 (typ)	(1.34V in TX mode)
	40	Bias 1	1.50 (typ)	(3.20V in TX mode)
	41	Modulation output	3.42 (typ)	(1.62V typ in TX mode)
	42	CCOMP (NU)	0.05	
	43	Steering line IOUT	9.62 (typ)	Depends on frequency
	44	PD ground	GND	
	45	Steering line IADAPT	9.62 (typ)	Depends on frequency
	46	Adapt switch (NU)	0	
	47	Voltage from charge pump	12.8	
	48	AUX1 output (NU)	2.98	
U251 VCO / Buffer	1	TX VCO current adjust	4.50	
	2	RX VCO current adjust	4.35	
	3	Superfiltered input	4.51	
	4	Collector RF in amp	4.35	
	5	RX VCO base	1.27	
	6	RX VCO emitter	0.48	
	7	RX switch output (NU)	0	
	8	RX buffered VCO output	3.36	
	9	GND_FLAG	GND	
	10	TX buffered VCO output	3.36	
	11	GND_BUFFERS	GND	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U251 VCO / Buffer	12	Prescaler output	2.26	
	13	TX switch output (NU)	0.06	
	14	Vcc_BUFFERS	3.00	
	15	TX VCO emitter	0	(RX mode)
	16	TX VCO base	0	(RX mode)
	17	GND_LOGIC	GND	
	18	Vcc_LOGIC	3.00	
	19	TRB input	0.03	From U201-2 (RX mode)
	20	FLIP input	GND	
U310 5V Regulator	1	Vin	7.48	
	2	Ground	GND	
	3	Control input	7.48	
	4	Bypass capacitor	1.26	
	5	Vout	4.96	
U320 3.3V Regulator	1	Ground	GND	
	2	Feedback	1.23	
	3	Tap (NU)	0	
	4	Vin	7.48	
	5	Vout	3.23	
	6	Sense (NU)	0	
	7	Error (reset output)	3.20	
	8	Shutdown input	7.48	
U330 3V Regulator	1	Vin	7.48	
	2	Ground	GND	
	3	Control input	7.48	
	4	Bypass capacitor	1.26	
	5	Vout	3.00	
U401 Microprocessor	1	PD4_SCK serial clock input	0	
	2	PD5_SS	3.23	ASFIC chip select
	3	PD6_VLIN	3.23	EEPROM chip select
	4	PG7_R_W	3.21	
	5	PG6_AS	3.23	
	6	PG0_XA13	3.23	
	7	PB7_ADDR15	0.026	
	8	PB6_ADDR14	0.028	
	9	PB3_ADDR11	3.06	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	10	PB1_ADDR9	3.05	
	11	PB2_ADDR10	0.16	
	12	VDD	3.23	
	13	VSS	GND	
	14	PBO_ADDR8	3.05	
	15	PB5_ADDR13	0.13	
	16	PG1_XA14	0.20	
	17	PG4_XA17	3.17	
	18	PG5_XA18	0	
	19	PG3_XA16	3.21	
	20	PG2_XA15	0.30	
	21	PB4_ADDR12	0.22	
	22	PF7_ADDR7	3.03	
	23	PF6_ADDR6	3.08	
	24	PF5_ADDR5	3.06	
	25	PF4_ADDR4	0.16	
	26	PF3_ADDR3	0.26	
	27	PF2_ADDR2	3.06	
	28	PF1_ADDR1	3.06	
	29	PFO_ADDR0	3.05	
	30	PC0_DATA0	0.69	
	31	PC1_DATA1	0.96	
	32	PC2_DATA2	1.10	
	33	PC3_DATA3	0.81	
	34	PC4_DATA4	0.62	
	35	PC5_DATA5	0.68	
	36	PC6_DATA6	0.67	
	37	PC7_DATA7	0.73	
	38	PH7_CSPROG	3.05	
	39	VDDL	3.23	
	40	VSSL	GND	
	41	PH6_CSGP2	3.23	
	42	PH5_CSGP1	3.23	
	43	PH4_CSIO	0	
	44	PH3_PW4	3.21	On/off control output
	45	PH2_PW3	0	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	46	PH1_PW2	3.00	
	47	PH0_PW1	3.23	Synth chip select
	48	XIRQ	3.00	
	49	PI7	1.48	RX enable
	50	PI6	0.01	TX enable
	51	PI5	3.23	
	52	PI4	0	Green LED enable
	53	PI3	0	Red LED enable
	54	PI2	0	
	55	PI1	0	
	56	PI0	2.98	Lock detect from U201-4
	57	MODB_VSTBY	3.22	Boot mode enable
	58	MODA_LIR	3.12	
	59	AVDD	3.23	
	60	PE7_AN7	3.20	
	61	PE6_AN6	3.20	
	62	PE5_AN5	2.91	VOX threshold detect
	63	PE4_AN4	0.73	RSSI input
	64	PE3_AN3	0.14	
	65	PE2_AN2	1.62	
	66	PE1_AN1	0 - 3.3 V	Volume control wiper
	67	PE0_AN0	2.48	33% of battery voltage
	68	VRL	0	
	69	VRH	3.20	
	70	AVSS	GND	
	71	PJ0_CSGP3	3.23	Side PTT button
	72	PJ1_CSGP4	0	External MIC PTT
	73	PJ2	3.23	
	74	PJ3	3.23	
	75	PJ4	3.23	
	76	PJ5	0	
	77	PJ6	3.23	Bottom option button
	78	PJ7	3.23	Top option button
	79	PA0_IC3	0	
	80	PA1_IC2	1.57	
	81	PA2_IC1	3.00	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	82	PA3_IC4_OC5_OC1	3.00	
	83	PA4_OC4_OC1	0	Squelch detect input
	84	PA5_OC3_OC1	0	Channel activity input
	85	PA6_OC2_OC1	0	
	86	PA7_PA1_OC1	0	
	87	VSSR	GND	
	88	VDDR	3.23	
	89	ECLK (NU)	1.60	
	90	EXTAL	1.70	Clock from U451-28
	91	XTAL	1.40	Not used
	92	VDDSYN	0	
	93	XFC (NU)	0	
	94	RESET	3.20	From U320
	95	LVOUT	0	
	96	IRQ	3.20	
	97	PD0_RXD	3.23	
	98	PD1_TXD	1.9	
	99	PD2_MISO	0	
	100	PD3_MOSI	3.23	
U402 EEPROM	1	Chip select	3.23	From U401-3
	2	Serial data out	0	
	3	Write protect	3.23	
	4	Vss	GND	
	5	Serial data in	3.23	
	6	Serial clock	0	
	7	Hold	3.23	
	8	Vcc	3.23	
U404 Flash ROM	1	A11	3.06	
	2	A9	3.08	
	3	A8	3.05	
	4	A13	0.13	
	5	A14	0.31	
	6	NC	3.17	
	7	EN_WE	3.21	From U401-4
	8	Vcc	3.23	
	9	RESET	3.20	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U404 Flash ROM	10	A16	3.17	
	11	A15	0.30	
	12	A12	0.22	
	13	A7	3.03	
	14	A6	3.08	
	15	A5	3.06	
	16	A4	0	
	17	A3	0.24	
	18	A2	3.08	
	19	A1	3.05	
	20	A0	3.05	
	21	D0	0.69	
	22	D1	0.94	
	23	D2	1.08	
	24	GND	GND	
	25	D3	0.78	
	26	D4	0.59	
	27	D5	0.66	
	28	D6	0.67	
	29	D7	0.75	
	30	EN_CE	3.01	From U401-38
	31	A10	0.16	
	32	EN_OE	0	From U401-86
U451 ASFIC_CMP	1	VDD for analog circuits	3.00	
	2	DISC audio input	1.34	From U510
	3	Ground for analog circuits	GND	
	4	DACU output	0	
	5	DACR output	0	
	6	DACG output	2.38 (typ)	Power set (TX mode)
	7	VOX peak detector output	2.91	
	8	PLCAP for DC integrator	0.40	
	9	SQIN	0.01	
	10	Universal audio input/output	0	
	11	VDD for DACs	4.95	
	12	SQCAP	0	
	13	GCB2 general purpose output	0	Audio PA_EN (unsquelched)

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U451 ASFIC_CMP	14	GCB1 general purpose output	0	
	15	GCB0 general purpose output	3.00	BW select (25 kHz mode)
	16	Squelch channel activity output	0	To U401-84
	17	Squelch detect digital output	0	To U401-83
	18	PL/low speed data I/O	1.50	
	19	High speed data I/O	3.00	
	20	Chip select	3.23	From U401-2
	21	Serial clock input	0	
	22	Serial data input	3.23	
	23	Ground for clock synthesizer	GND	
	24	Loop filter cap for clock syn	0.74	
	25	PLCAP2 for LS integrator	1.17	
	26	Not used	0	
	27	Vdd for clock synthesizer	3.00	
	28	Clock synthesizer output	1.70	
	29	1200 Hz ref for MDC decode	3.00	
	30	GNDDO	GND	
	31	Ground for digital circuits	GND	
	32	Vdd for analog switches	4.96	
	33	Vdd for digital circuits	3.00	
	34	16.8 MHz master clock input	1.54	
	35	GCB3 general purpose output	3.00	Internal MIC enable
	36	TX audio return from option	0	
	37	GCB4 general purpose output	0	
	38	GCB5 general purpose output	0	
	39	RX audio send to option	1.48	
	40	Modulation output	1.50	To U201-10
	41	RX audio out to power amp	1.51	
	42	Flat TX audio return from option	0.20	
	43	RX audio return to option	1.50	
	44	Flat TX audio send to option	1.50	
	45	Vdd for audio path I/O filters	3.00	
	46	Mic audio input	1.50	
	47	Ground for audio path I/O filters	GND	
	48	Ext mic audio input (not used)	0	

Table 12-4. Troubleshooting Table for Board and IC Signals (Continued)

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U480 Dual Opamp	1	Unit 1 output	2.48	
	2	Unit 1 (-) input	2.48	
	3	Unit 1 (+) input	2.46	
	4	Ground	GND	
	5	Unit 2 (+) input	0.28	
	6	Unit 2 (-) input	0.29	
	7	Unit 2 output	0	
	8	Vcc	4.96	
U490 Audio Power Amp	1	Enable/shutdown	0.12	(Unsquelched)
	2	Bias reference	3.26	(Unsquelched)
	3	(+) input	3.26	(Unsquelched)
	4	(-) input	3.27	(Unsquelched)
	5	(-) output	3.25	(Unsquelched)
	6	Vcc	7.48	(Unsquelched)
	7	Ground	GND	
	8	(+) output	3.29	(Unsquelched)
U510 Dual Opamp	1	Unit 1 output	1.75	
	2	Unit 1 (-) input	1.56	
	3	Unit 1 (+) input	1.55	
	4	Ground	GND	
	5	Unit 2 (+) input	1.55	
	6	Unit 2 (-) input	1.56	
	7	Unit 2 output	1.38	
	8	Vcc	4.96	

1. All voltages are measured with a high-impedance digital voltmeter and expressed in volts DC relative to ground (0V).
2. Voltages are measured with a DC input voltage of 7.50 + .02 volts DC applied to the battery connector (J301).
3. All voltages are measured in the squelched receive mode, unless otherwise indicated.
4. Voltages are identical for VHF and UHF models unless otherwise indicated.

Notes:

Chapter 13 UHF Schematic Diagrams, Overlays, and Parts Lists

13.1 Introduction

This section provides schematic diagrams, overlays, and parts lists for the radio circuit boards and interface connections.

13.1.1 Notes For All Schematics and Circuit Boards

* Component is frequency sensitive. Refer to the Electrical Parts List for value and usage.

1. Unless otherwise stated, resistance values are in ohms (K = 1000), capacitance values are in picofarads (pF) or microfarads (µF), and inductance values are in nanohenries (nH) or microhenries (µH).
2. DC voltages are measured from point indicated to chassis ground using a Motorola DC multimeter or equivalent. If the board has been removed from the chassis, the transmitter module mounting screws may be used for ground connection. (*Note: The antenna nut bracket is not connected to ground.*) Operating mode dependent voltages are followed by (RX) for receive mode, (TX) for transmit mode, (UNSQ) for unsquelched mode, etc.
3. RF voltages on VHF models are measured with a Fluke model 85 RF probe. The indicated voltages expressed in mV (RF) are DC level readings which correspond approximately 1:1 to the RF voltage level in mV rms. RF voltages in the Receiver Front End and Receiver Back End circuits are measured with an on-channel 100 mV (-7 dBm) RF signal applied to the antenna jack J140.
4. RF voltages on UHF models are measured both with a high-impedance RF voltmeter having a bandwidth in excess of 500 MHz (levels are expressed in dBm) and with a Fluke model 85 RF probe [levels are expressed in mV (RF)]. These indicated voltages are DC level readings which correspond approximately 1:1 to the RF voltage level in mV rms, and are only approximate for UHF frequency measurements. RF voltages in the Receiver Front End and Receiver Back End circuits are measured with an on-channel 100 mV (-7 dBm) RF signal applied to the antenna jack J140.
5. Audio voltages are measured with a high-impedance AC rms voltmeter. The indicated voltages are expressed in mV rms. Receive mode voltages are followed by (RX) and are measured with an on-channel signal with 1 kHz modulation at 60% deviation (3 kHz for 25 kHz channels, or 1.5 kHz for 12.5 kHz channels). Transmit mode voltages are followed by (TX) and are measured with a 1 kHz, 10 mV rms signal present at the external microphone input (accessory connector J471 pin 4 hot and pin 7 ground).
6. Reference Designators are assigned in the following manner:

Ref. No. Series	Circuit Block
1-99	RF Front End
100-149	Transmitter RF Stages
150-200	Transmitter Power Control
201-250	Frequency Synthesizer
251-300	VCO

Ref. No. Series	Circuit Block
301-400	DC Regulation
401-450	Microprocessor
451-550	Audio

7. Circuit Block Interconnection Legend:

Name	Description
USWB+	Unswitched Battery Voltage (always on)
5V	5 volts (regulated)
5R	5 volts in RX mode only
5T	5 volts in TX mode only
RESET	Low-line reset signal from U320 to uP
D3_3V	Digital 3.3 volts (regulated)
3V	Analog 3 volts (regulated)
TX_ENA	Transmit enable signal from uP to transmitter
PWR_SET	DC voltage from ASFIC to TX power control
DEMOD	RX audio from backend to ASFIC
BW_SEL	Backend filter BW select from ASFIC
RSSI	RX signal strength indication from IFIC to uP
IF_IN/OUT	44.85 MHz from 1st mixer to high IF filter
RF_IN/OUT	RX signal from antenna switch to front end
MOD OUT/IN	TX modulation from ASFIC to synthesizer
16_8_MHZ	Ref osc signal from synthesizer to ASFIC
SYNTH_CS	Synthesizer chip select from uP
SPI_CLK	Serial clock from uP
SPI_DATA_OUT	Serial data from uP
LOCK	Lock detect indication from synth to uP
PRESC	VCO freq feedback from VCOBIC to synth
V_STEER	Steering line voltage from synth to VCO's
V_SF	Super-filtered 4.5 volts from synth to VCOBIC
VCO_MOD	TX modulation from ASFIC to synthesizer
TRB	TX/RX control from synth to VCOBIC
RX_INJ	Buffered RX VCO output to RX 1st mixer
TX_INJ	TX VCO output to transmitter input

13.1.2 Six Layer Circuit Board

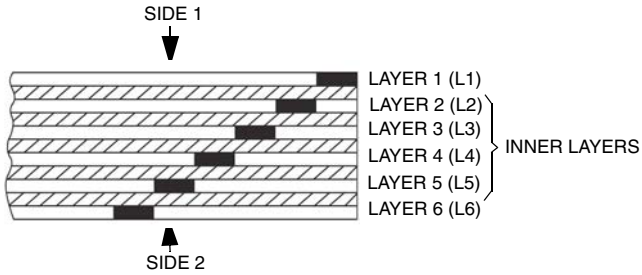

Figure 13-1. Six-Layer Circuit Board: Copper Steps in Layer Sequence

13.2 Speaker and Microphone Schematic

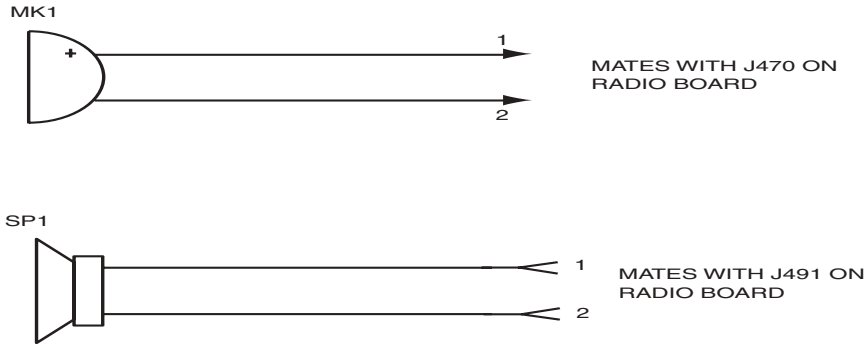

Figure 13-2. Speaker and Microphone Schematic

13.2.1 Speaker and Microphone Parts List

Reference Designator	Motorola Part No.	Description
MK1	5085880L01	Microphone, electret
SP1	5085738Z08	Speaker assembly with connector

Notes:

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Notes:

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